

SiGe/Si MONOLITHICALLY INTEGRATED AMPLIFIER CIRCUITS

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Introduction

With recent advance in the epitaxial growth of silicon-germanium heterojunction, Si/SiGe HBTs with high f_{\max} and f_T [1][2] have received great attention in MMIC applications [3][4]. In the past year, technologies for mesa-type Si/SiGe HBTs and other lumped passive components with high resonant frequencies have been developed and well characterized for circuit applications. By integrating the micromachined lumped passive elements into HBT fabrication, multi-stage amplifiers operating at 20 GHz have been designed and fabricated.

Si/SiGe HBTs

To implement MMICs, active devices are the most crucial components that determine the overall performance of microwave circuits. The HBT structure shown in Fig. 1 starts from Si substrate with a resistivity of $\rho \sim 10 \text{ k}\Omega\text{cm}$. First, As-doped subcollector is formed by chemical vapor deposition, then the other epitaxial layers are grown by MBE. The growth temperature is fixed at 415 °C for the collector and emitter layers, and 550 °C for the base layer. Emitter and collector layers are Sb-doped Si, while the base layer is B-doped SiGe alloy with a uniform Ge mole fraction of 40%. The doping concentration and thickness of the base layer are $2 \times 10^{19} \text{ cm}^{-3}$ and 200 Å, respectively. Unintentionally doped spacer layers are inserted at E-B and B-C junction to minimize the effect of boron outdiffusion.

Mesa-type HBTs have been fabricated with a standard lift-off and etching techniques. Emitter contact is formed by a Cr/Au metal layer, while base and collector contacts are made with Pt/Au and Ti/Au, respectively. Rapid thermal annealing (RTA) is performed after metal deposition to reduce the contact resistance of these electrodes. Base and collector mesa are formed with SF_6 and O_2 -based reactive ion etch (RIE). Emitter mesa formation, which exposes the base layer for metallization, is the most critical step in the fabrication process of mesa-type HBTs since this process directly affects the f_{\max} of the devices through the parasitic base resistance R_B . Over-etching of the base layer and undercutting of emitter layer should be minimized to keep the value of R_B small. To achieve this, we use a two-step etch. First, an anisotropic RIE step removes most of the emitter layer without undercut. Second, a KOH-based solution selectively etches the remaining emitter layer and stops close to the E-B junction. This also introduces minimal undercut for self-aligned base metal deposition. SiO_2 passivation, via hole formation, and interconnection metal deposition for probe pads complete the whole process.

DC and RF characteristics of the Si/SiGe HBTs have been measured and analyzed. The devices have

n+ Si	emitter contact	$2 \times 10^{19} \text{ cm}^{-3}$	2000 Å
n Si	emitter	$2 \times 10^{18} \text{ cm}^{-3}$	1000 Å
i $\text{Si}_{0.6}\text{Ge}_{0.4}$			50 Å
p+ $\text{Si}_{0.6}\text{Ge}_{0.4}$	base	$2 \times 10^{19} \text{ cm}^{-3}$	200 Å
i $\text{Si}_{0.6}\text{Ge}_{0.4}$			50 Å
n- Si	collector	$5 \times 10^{15} \text{ cm}^{-3}$	3000 Å
n+ Si	sub-collector	$1 \times 10^{19} \text{ cm}^{-3}$	15000 Å
p- Si	substrate	$1 \times 10^{12} \text{ cm}^{-3}$	540 μm

Figure 1. Si/SiGe HBT material structure

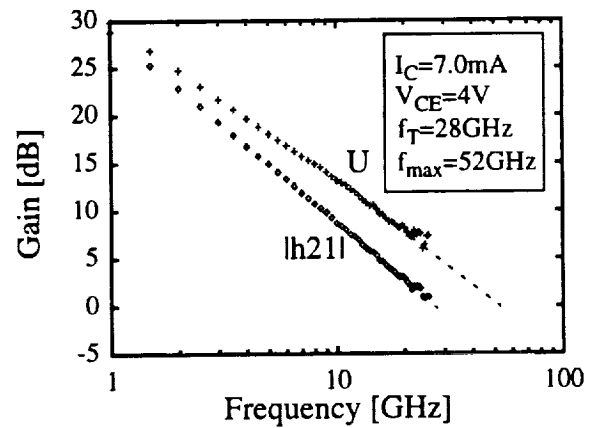


Figure 2. Frequency response of Si/SiGe HBT ($A_E = 5 \times 5 \mu\text{m}^2$)

Paper List for NASA Si/SiGe Project

Journal Papers:

1. J.-S. Rieh, O. Qasaimeh, L.-H. Lu, K. Yang, L.P.B. Katehi, P. Bhattacharya and E.T. Croke, "Single- and Dual-Feedback Transimpedance Amplifiers Implemented by SiGe Technology," *Microwave and Guided Wave Letters*, **8** (2), February 1998.
2. J.-S. Rieh, D. Klotzkin, O. Qasaimeh, L.-H. Lu, K. Yang, L.P.B. Katehi, P. Bhattacharya and E.T. Croke, "Monolithically Integrated Single- and Multiple-channel SiGe/Si PIN-HBT Front-End Transimpedance Photoreceivers," *Photonics Technology Letters*, **10** (3), March 1998.
3. J.-S. Rieh, L.-H. Lu, L.P.B. Katehi, P. Bhattacharya, E.T. Croke G.E. Ponchak and S.A. Alterovitz, "X- and Ku-band Amplifiers Based on Si/SiGe HBTs and Micromachined Components," *Transactions on Microwave Theory and Techniques*, accepted for publication.

Conference Papers:

1. L.-H. Lu, J.-S. Rieh, P. Bhattacharya, L.P.B. Katehi, E.T. Croke, G.E. Ponchak and S.A. Alterovitz, "K-band Si/SiGe HBT MMIC Amplifiers Using Lumped Passive Components with a Micro Machined Structure," submitted to 1998 IEEE RFIC Symposium.
2. J.-S. Rieh, O. Qasaimeh, D. Klotzkin, L.-H. Lu, K. Yang, L.P.B. Katehi, P. Bhattacharya and E.T. Croke, "Monolithically Integrated SiGe-Based PIN-HBT Front-End Transimpedance Photoreceivers," Proceedings 1997 IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, pp. 322-331, 1997.

Report on SiGe/Si Monolithically Integrated Circuits

by

Liang-hung Lu and Jae-sung Rieh

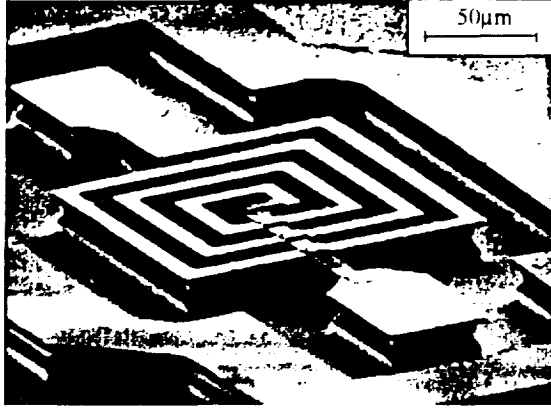


Figure 4. Photomicrograph of the micromachined spiral inductor

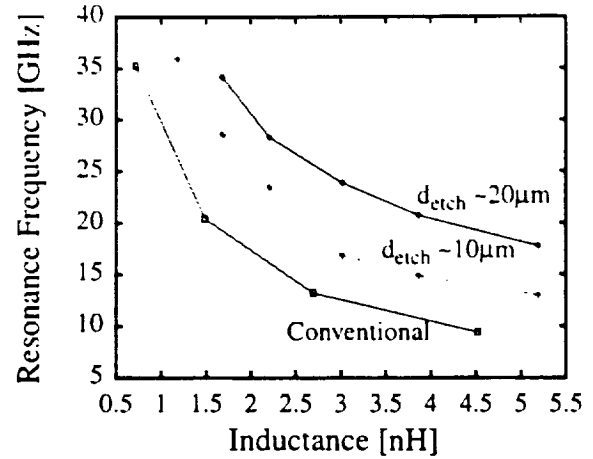


Figure 5. Resonant frequencies of inductors with various etch depth, d_{etch} .

HBT Amplifier Design

After fabrication and characterization of active devices and passive components, the measured s-parameters and equivalent circuits are used for amplifier design. Using coplanar waveguides, one-stage, two-stage and three-stage lumped amplifiers are designed at a center frequency of 20 GHz. Figure 6 shows the lumped amplifiers. In the designs, micromachined passive components are used for input, output and inter-stage matchings to optimize the gain and remain the amplifiers in stable region. In addition, DC bias pads and RF chokes are also included in the design.

Future Work

The next step for the work is to complete the fabrication of the amplifiers and take measurement data. Then we propose to develop a new HBT technology for active devices with higher RF performance, and use the improved devices for circuit applications at higher frequencies.

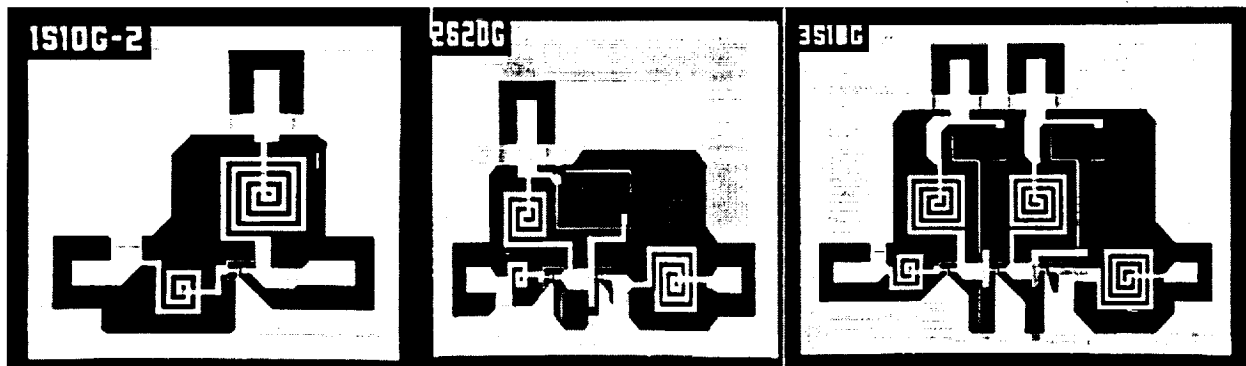


Figure 6. Photomicrograph of the fabricated amplifiers.

K-band Si/SiGe HBT MMIC Amplifiers Using Lumped Passive Components with a Micromachined Structure.

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Abstract

Using Si/SiGe heterojunction bipolar transistors with a maximum oscillation frequency of 52 GHz and a novel structure for passive components, a two-stage K-band lumped-element amplifier has been designed and fabricated on high-resistivity Si substrates. The chip size including biasing and RF chokes is $0.92 \times 0.67 \text{ mm}^2$.

Introduction

With recent advances in the epitaxial growth of silicon-germanium heterostructures, the concept of high-performance and high-frequency electronic devices compatible with advanced silicon technology has been realized. The Si/SiGe heterojunction bipolar transistors (HBTs) have received the greatest attention[1][2]. Recently, monolithic microwave and millimeter wave integrated circuits (MMICs) based on Si/SiGe HBTs and distributed circuit components have been presented[3][4].

In this work, we have developed the fabrication technologies for Si/SiGe HBT on high-resistivity Si substrates. For a $5 \times 5 \text{ } \mu\text{m}^2$ emitter size, a 28 GHz cut-off frequency and a maximum oscillation frequency of 52 GHz was demonstrated. In addition, lumped coplanar novel micromachined passive components characterized by high resonant frequencies are also modeled and fabricated. By integrating these passive components into the HBT fabricating process, the application range of Si MMICs with lumped elements can be extended even above 30 GHz. K-band lumped amplifiers using these micromachined passive components

have been designed and fabricated based on the Si/SiGe HBTs.

Si/SiGe HBTs

Active devices are the most crucial components that determine the overall performance of microwave circuits. Optimized structure, high quality epitaxial layers, and stable processing technology are the key to successful development of high performance devices for high-frequency circuit applications. We have designed and grown npn double heterojunction Si/SiGe HBT structures by molecular beam epitaxy (MBE). The HBT structure is shown in Fig. 1. The substrate is Si with a resistivity of $\rho \sim 10 \text{ k}\Omega\text{cm}$, which is high enough to suppress the substrate-originated ohmic loss for passive components in microwave circuit applications[5]. First, As-doped subcollector is formed by chemical vapor deposition, then the other epitaxial layers are grown by MBE. The growth temperature is fixed at 415°C for the collector and emitter layers, and 550°C for the base layer. Emitter and col-

n+ Si	emitter contact	$2 \times 10^{19} \text{ cm}^{-3}$	2000 Å
n Si	emitter	$2 \times 10^{18} \text{ cm}^{-3}$	1000 Å
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p- Si	substrate	$1 \times 10^{12} \text{ cm}^{-3}$	540 μm

Figure 1. Si/SiGe HBT material structure

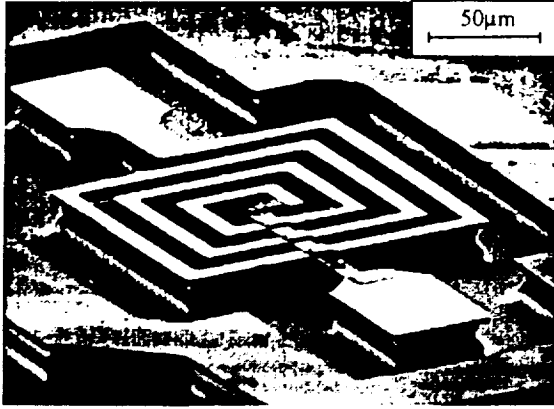


Figure 4. Photomicrograph of the micromachined spiral inductor

sion line elements, lumped elements are smaller, especially at frequencies below 30 GHz. As a result, lumped element circuits can be more compact than distributed ones in MMIC applications. However, planar lumped elements suffer from parasitic capacitance. Specifically, planar lumped inductors exhibit very low resonant frequencies due to the parasitic capacitance, thus limiting operating frequencies. Work has been done by fabricating the inductors on dielectric membrane to increase the resonant frequency[6][7]. This approach is difficult to be integrated with active devices since it requires the development of a dielectric membrane between the bulk high-resistivity Si and the doped layers. To avoid this difficulty, a new micromachined spiral inductor has been developed as shown in Fig. 4. By covering the metal structure with Ni which is used as a self-aligned mask and removing the substrate material in between the turns by RIE, the effective dielectric constant of this structure can be reduced. This results in a smaller series and shunt parasitic capacitance from turn to turn and from the signal line to ground. Due to the significant reduction of the parasitics, the resonant frequency can be increased drastically. In the measurement, the resonant frequency increases from 20 GHz to 38 GHz for a 1.5 nH spiral inductor by using this micromachined structure. The complete measurement results for the micromachined spiral inductors with various inductance and etching depth are shown in Fig. 5. Other passive components are also integrated into the processes and modeled for the circuit design. A 2000 Å SiO layer is used as the

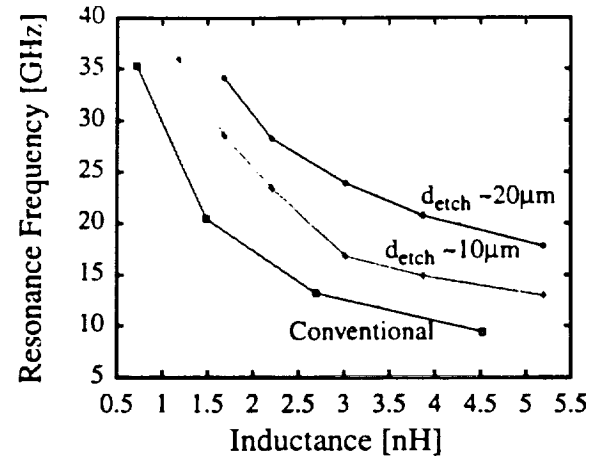


Figure 5. Resonant frequencies of inductors with various etch depth, d_{etch} .

dielectric material for MIM capacitors. The extracted dielectric constant ϵ_r is 4.7 which provides a capacitance of $0.21 \text{ fF}/\mu\text{m}^2$. For thin film resistors (TFRs), a NiCr layer of 700 Å is used and gives a sheet resistance of $25\text{--}30 \Omega/\square$.

HBT Amplifier Circuits

Using coplanar waveguides, a two-stage lumped amplifier as shown in Fig. 6 is designed and fabricated. It consists two $5 \times 5 \mu\text{m}^2$ Si/SiGe HBTs. Micromachined spiral inductors, MIM capacitors and TFRs are used for the matching network, transistor biasing and RF blocks, and the

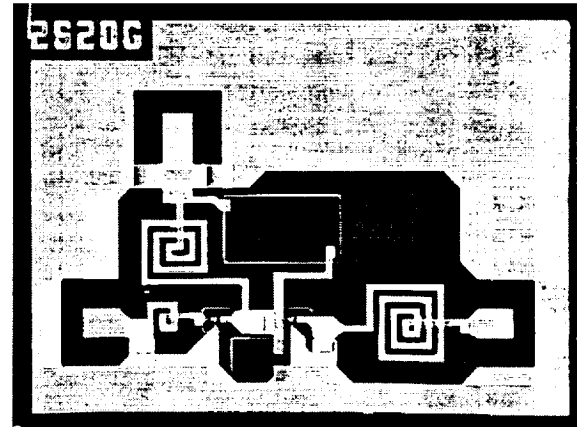


Figure 6. Photomicrograph of the fabricated two-stage amplifier. The chip size is $0.92 \times 0.67 \text{ mm}^2$

Single- and Dual-Feedback Transimpedance Amplifiers

Implemented by SiGe HBT technology

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ABSTRACT

Monolithically integrated SiGe/Si heterojunction bipolar transistor transimpedance amplifiers, with single- and dual-feedback configurations, have been designed, fabricated, and characterized. The single-feedback amplifier showed transimpedance gain and bandwidth of 45.2 dB Ω and 3.2 GHz, respectively. The dual-feedback version exhibits improved gain and bandwidth of 47.4 dB Ω and 3.3 GHz, respectively. Their performance characteristics are excellent in terms of their application in communication systems.

I. Introduction

Fiber optical communication systems have been dominated by III-V based devices and circuits due to their superior properties over Si, such as high speed operation, bandgaps corresponding to the long-haul fiber compatible 1.3 μm or 1.55 μm wavelength, and light emitting capability [1,2]. Recent rapid developments in SiGe/Si technology seems to be able to satisfy many requirements of fiber optical communication systems in terms of both performance and cost. Current SiGe/Si heterojunction bipolar transistors (HBTs) demonstrate operating frequencies high enough for next generation fiber optical communication systems [3,4]. The bandgap of $\text{Si}_{1-x}\text{Ge}_x$ alloys can coincide with the wavelength of 1.3 μm or 1.55 μm by proper choice of Ge mole fraction [5]. SiGe/Si quantum dot light emitting diodes have been reported, albeit the devices are in an early stage of development [6]. This letter reports experimental results of SiGe/Si HBT-based single- and dual-feedback transimpedance amplifiers, which can be employed as a preamplifier in a front-end photoreceiver of a fiber optical communication receiver module.

II. Fabrication

The schematic of the SiGe/Si n-p-n HBT, grown by molecular beam epitaxy (MBE) is shown in Fig. 1. $\text{Si}_{1-x}\text{Ge}_x$ alloy was employed as a thin base layer with the Ge mole fraction graded from $x=0.1$ (emitter side) to $x=0.4$ (collector side). This grading of Ge composition generates a quasi-electric field which accelerates electrons travelling through the base to collector, resulting in smaller base transit time and eventually higher cutoff frequency compared with a uniform Ge composition profile. The fabrication procedure for mesa-type SiGe HBTs is as follows: emitter metal (Cr/Au=500/2000 \AA) is

defined by evaporation on the Si contact layer and used as a mask for the subsequent KOH-based selective wet etching which exposes the base layer for contact formation. Evaporation of the self-aligned base metal(Pt/Au=200/1300 Å) follows, and then base and collector layers are removed by dry etching to expose the highly doped subcollector layer for collector contact. Collector metal(Ti/Au=500/2000 Å) is deposited by evaporation on the exposed subcollector layer, and another dry etching is performed for the device isolation. SiO₂ layer is deposited by PECVD and via holes for contacts are formed by selective dry etching of the SiO₂ layer. Evaporation of thick interconnection metal(Ti/Al/Ti/Au=500/11000/500/3000 Å) concludes the device fabrication. The process described above leads to high yield and good device characteristics. From the current-voltage characteristics of devices with 2.5 µm×10 µm emitter size, a DC current gain β is measured 25. The S-parameters were measured with HP8510 network analyzer in the 0.5 GHz-25.5 GHz frequency range. Values of f_T and f_{max} , obtained from the extrapolation of the values of current gain h_{21} and unilateral power gain U at 20 GHz with the assumption of -6dB/octave roll-off, are 23 GHz and 34 GHz, respectively. Two additional processing steps are required to complete amplifier fabrication: formation of thin film resistors and airbridges. NiCr was evaporated(700 Å) and used as resistors, with measured sheet resistance of 25 Ω/□. Evaporated metal(Ti/Al/Ti/Au=500/14000/500/3000 Å) was used to form airbridges.

III. Results and Discussion

Figure 2(a) shows the circuit diagram of the single-feedback transimpedance amplifier. It consists of a common emitter gain stage, two emitter follower buffers, a

resistive feedback loop, and a front-end inductor. The feedback resistor R_F is the most important component in this configuration since it determines the bandwidth, gain, and noise characteristics of the whole circuit. The value of this resistor should be selected based on trade-off between these parameters. It is generally known that the increase of R_F increases the gain and improves the noise characteristics, while degrading the bandwidth of the circuit. In this study, the value of R_F was chosen to be $550\ \Omega$, with slightly more emphasis on the bandwidth. The inclusion of front-end inductor L_1 has been shown to improve the signal-to-noise ratio and enhance the bandwidth of the amplifier[1]. The circuit diagram of the dual-feedback amplifier is shown in Fig. 2(b). It includes a second gain stage following the first one, and an extra feedback loop including a resistor R_{F2} , allowing R_{E1} to behave as a voltage feedback. This second feedback, along with the reduced value of R_{F1} ($200\ \Omega$), increases the bandwidth of the amplifier. The gain would be reduced due to the additional feedback configuration, but the additional gain from the second gain stage compensates for the reduction and provides an increase of overall gain-bandwidth product of the amplifier compared with the single-feedback amplifier.

The S-parameters of the fabricated amplifiers were measured with a HP8510 network analyzer in the 0.1 GHz-10.0 GHz frequency range. Figure 3(a) shows the transimpedance gain versus frequency characteristics of a single-feedback amplifier circuit. It shows a transimpedance gain of $45.2\ \text{dB}\Omega$ and -3 dB bandwidth of 3.2 GHz at the bias point $V_{CC}=3\ \text{V}$. The gain shows uncharacteristic ripples in the high frequency range, which arise from the external bias probing in on-wafer measurement. The measured bandwidth is slightly enhanced by this ripple and the real value is conservatively estimated to be around 3 GHz. A moderate gain overshoot can be seen in the gain plot. This

is ascribed to the parasitic inductance arising from the narrow coplanar ground line surrounding the whole circuit. The frequency response of a dual-feedback amplifier is shown in Fig. 3(b). The transimpedance gain is $47.4 \text{ dB}\Omega$ and the -3 dB bandwidth is measured to be 3.3 GHz at the bias point of $V_{CC}=7 \text{ V}$. This circuit shows improvement in both gain and bandwidth compared with the single-feedback version. These performance characteristics are comparable to III-V based-circuit of the same complexity[7] and indicate the possibility of applying SiGe technology to fiber optical communication systems with the advantages of low cost and simpler fabrication. Increase of V_{CC} affected both gain and bandwidth, leading to an increase of gain and decrease of bandwidth. A similar trend was observed for the single-feedback amplifier. This effect gives rise to another degree of freedom for achieving a trade-off between gain and bandwidth and allows a post-fabrication tuning of gain and bandwidth, which may compensate for the possible deviation of these parameters from designed values due to process variation.

ACKNOWLEDGEMENT

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lithic p-i-n/HBT photoreceiver module for long-wavelength transmission systems",
IEEE Photon. Technol. Lett., vol. 7, pp. 182-184, Feb. 1995.

FIGURE CAPTIONS

Figure 1. Material structure of SiGe/Si HBTs

Figure 2. (a) Circuit diagram of single-feedback transimpedance amplifier

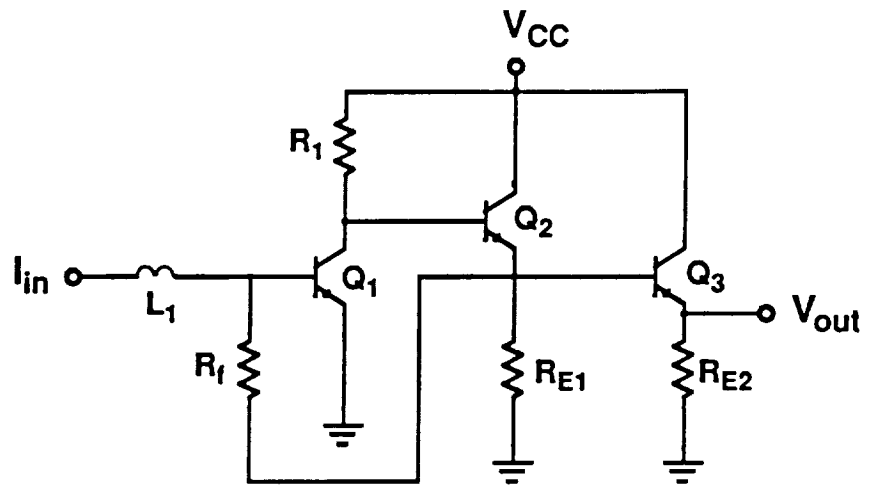
(b) Circuit diagram of dual-feedback transimpedance amplifier

Figure 3. (a) Frequency response of single-feedback transimpedance amplifier

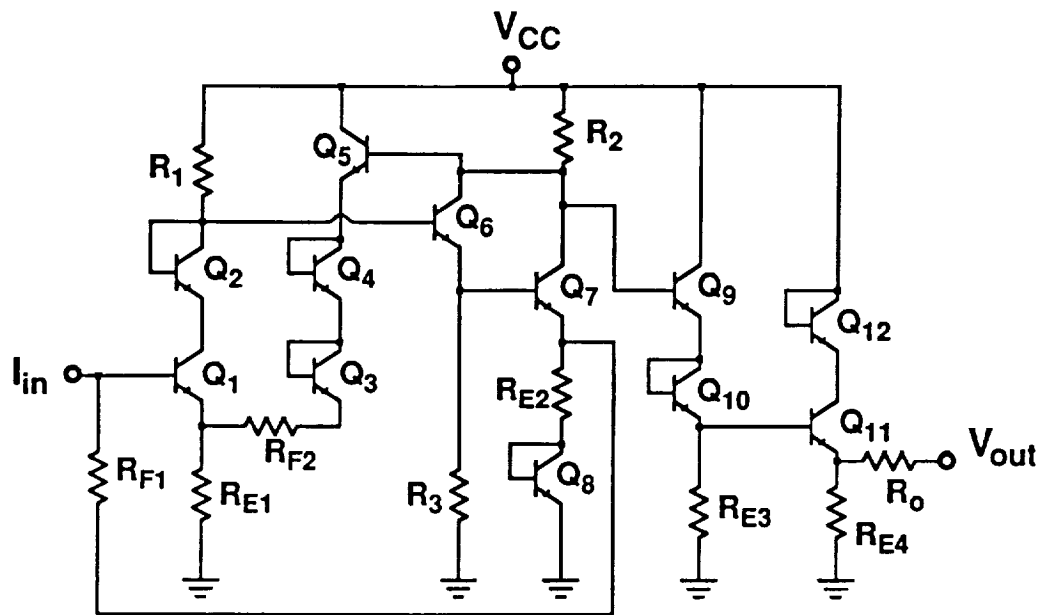
(b) Frequency response of dual-feedback transimpedance amplifier

Si	n+	1e19	200 nm
Si	n	2e18	100 nm
Si_{0.9}Ge_{0.1}	i		1 nm
Si_{1-x}Ge_x x:0.1→0.4	p+	5e19	30 nm
Si_{0.6}Ge_{0.4}	i		10 nm
Si	n-	1e16	250 nm
Si	n+	1e19	1.5 μm
Si Substrate	p-		

Figure 1

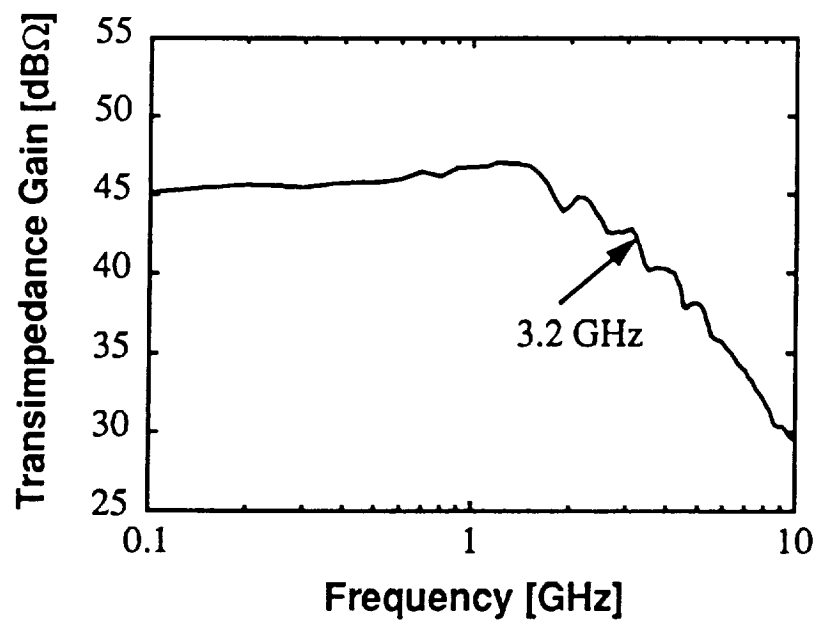


(a)

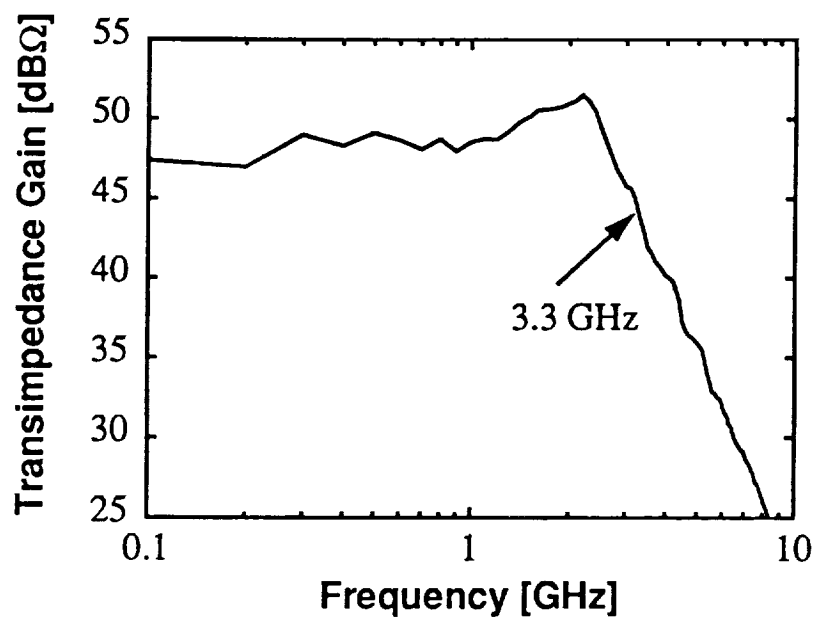


(b)

Figure 2



(a)



(b)

Figure 3

Monolithically Integrated SiGe/Si PIN-HBT Front-End Transimpedance Photoreceivers

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Abstract

The demand for monolithically integrated photoreceivers based on Si-based technology keeps increasing as low cost and high reliability products are required for the expanding commercial market. Higher speed and wider operating frequency range are expected when SiGe/Si heterojunction is introduced to the circuit design. In this paper, a monolithic SiGe/Si PIN-HBT front-end transimpedance photoreceiver is demonstrated for the first time. For this purpose, mesa-type SiGe/Si PIN-HBT technology was developed. Fabricated HBTs exhibit f_{\max} of 34 GHz with DC gain of 25. SiGe/Si PIN photodiodes, which share base and collector layers of HBTs, demonstrate responsivity of 0.3 A/W at $\lambda=850$ nm and bandwidth of 450 MHz. Based on these devices, single- and dual-feedback transimpedance amplifiers were fabricated and they exhibited the bandwidth of 3.2 GHz and 3.3 GHz with the transimpedance gain of 45.2 dB Ω and 47.4 dB Ω , respectively. Monolithically integrated single-feedback PIN-HBT photoreceivers were implemented and the bandwidth was measured to be ~ 0.5 GHz, which is limited by the bandwidth of PIN photodiodes.

I. Introduction

The commercial market for optical communication keeps expanding as modern society requires faster communication systems with higher capacity. In a large scale, long-haul fiber optical communication is spreading quickly and is ready for penetration into homes and offices. In a small scale, local optical data link is expected to replace electrical interconnection for high-speed computation and switching application[1]. As a result, the demand for components comprising optical communication systems is rising rapidly. To meet this huge demand, mass production is necessary and this requires a technology with low cost and high reliability. Till date, III-V based technology has primarily dominated these applications owing to its high-speed characteristics, superior optical properties, and feasibility to incorporate materials corresponding to 1.3 μm and 1.55 μm wavelength, which are required for long-haul fiber optical communication system based on silica optical fibers in terms of low dispersion and low loss,

Emitter Contact	Si	n+	1e19	200 nm
Emitter	Si	n	2e18	100 nm
Spacer	Si _{0.9} Ge _{0.1}	i		1 nm
Base	Si _{1-x} Ge _x x:0.1→0.4	p+	5e19	30 nm
Spacer	Si _{0.6} Ge _{0.4}	i		10 nm
Collector	Si	n-	1e16	250 nm
Subcollector	Si	n+	1e19	1.5 μ m
Substrate	Si	p-	2e12	540 μ m

Fig 1. Schematic of the SiGe PIN-HBT structure

respectively. The high-cost nature of III-V technology, however, remains a major impediment for it to be a favorable candidate for growing commercial applications which requires mass production. In contrast, Si-based technology benefits from its low cost and high reliability which is essential for commercial applications. There has been a lot of efforts to implement optical system components with Si technology, mainly for receiver modules. Such efforts started with hybrid approaches that combines III-V based photodiode to Si-based transimpedance amplifiers to make advantage of optical and high-speed properties of III-V materials and low cost nature of Si technology[2][3]. This approach, however, still suffers from its complexity and unreliability. Monolithic photoreceivers based on silicon, which eliminate the shortcomings of the hybrid realized by incorporating both photodiode and transimpedance amplifier on one chip, have been reported recently[4-7]. If the SiGe/Si heterostructure technology is incorporated to this monolithic approach, more advantages can be expected. SiGe/Si technology offers superior high speed characteristics than Si technology does, and it may be compatible with 1.3 μ m and 1.55 μ m wavelength by proper choice of Ge mole fraction in SiGe alloys while keeping the cost still low because it is basically based on existing matured Si technology. To the authors' knowledge, no SiGe based monolithic photoreceiver has been yet reported. In this paper, we report the development of SiGe/Si PIN-HBT technology and demonstrate the performance characteristics of transimpedance amplifiers and monolithically integrated PIN-HBT front-end transimpedance photoreceivers based on SiGe/Si heterostructures.

II. Fabrication

The schematic of the SiGe/Si PIN-HBT structure is shown in Fig. 1. A thick arsenic-doped subcollector layer is grown by CVD on (100) Si wafer with high resistivity ($\rho > 2000 \Omega\text{cm}$). Then the wafer is loaded into the MBE chamber, and antimony-doped Si collector layer,

boron-doped $\text{Si}_{1-x}\text{Ge}_x$ base layer, and antimony-doped Si emitter and emitter contact layer are grown. Unintentionally doped spacer layers are inserted in both sides of base to minimize the effect of boron outdiffusion. Ge mole fraction in the $\text{Si}_x\text{Ge}_{1-x}$ alloy incorporated as a base layer is graded from $x=0.1$ (emitter side) to $x=0.4$ (collector side) to generate a quasi-electric field. This field is intended to accelerate electrons travelling through the base to collector, resulting in smaller base transit time and eventually higher cut-off frequency compared to a uniform Ge composition profile. The fabrication procedure of the circuit begins with the deposition of emitter metal ($\text{Cr}/\text{Au}=500/2000 \text{ \AA}$) by evaporation on the Si contact layer. This layer is used as an etch mask for subsequent emitter mesa etch. Emitter mesa is formed with two step etch: dry and wet etch. First, SF_6 and O_2 -based anisotropic reactive ion etch (RIE) removes most portion of the emitter layer without undercut. Then, KOH-based selective wet etch is done to expose highly doped SiGe base layer with selectivity. This wet etch is accurately controlled to optimize the undercut for the minimization of the base access resistance and the successful formation of the following self-aligned base metal contact. Rapid thermal annealing (RTA) is done for the optimized ohmic contact of emitter metal in between two etch steps. Evaporation of the self-aligned base metal ($\text{Pt}/\text{Au}=200/1300 \text{ \AA}$) follows, and then base mesa is formed by RIE resulting in the exposure of the highly doped subcollector layer for collector contact. The base contact is also used as a p-contact for PIN photodiodes. Collector metal ($\text{Ti}/\text{Au}=500/2000 \text{ \AA}$) contact, also used as a n-contact for photodiode, is defined by evaporation on the exposed highly doped subcollector layer, and another RTA is performed for base and collector ohmic contact. A deep RIE is done to completely remove the subcollector layer between active devices for isolation, and SiO_2 layer ($1\mu\text{m}$) is deposited by PECVD for the separation of electrode metal contacts of the devices from following interconnection metal layer. This SiO_2 layer also behaves as a passivation layer for HBTs and an anti-reflection coating for photodiodes. Via holes for contacts are formed by selective dry etching of the SiO_2 layer, followed by the evaporation of thin film resistor ($\text{NiCr}=700 \text{ \AA}$). The measured sheet resistance of the resistors was around $25 \Omega/\square$. Thick interconnection metal ($\text{Ti}/\text{Al}/\text{Ti}/\text{Au}=500/11000/500/3000 \text{ \AA}$) deposition is followed for the formation of measurement probing pads. Finally, airbridges are formed for the formation of inductor feedlines and crossovers of metal layers by the evaporation of thick metal ($\text{Ti}/\text{Al}/\text{Ti}/\text{Au}=500/14000/500/3000 \text{ \AA}$).

III. Results and Discussion

The process described above leads to devices with high yield and excellent characteristics. From the current-voltage characteristics of HBTs with the emitter size of $2.5 \mu\text{m} \times 10 \mu\text{m}$, DC current gain β is measured to be 25 and the breakdown voltage to be 5 V. The collector and base ideality factors of the devices, extracted from its Gummel plot, are $n_c=1.12$ and $n_b=1.84$, respectively. The S-parameters were measured with a HP8510 network analyzer in the 0.5 GHz-25.5 GHz frequency range. Cut-off frequency f_T and maximum oscillation frequency

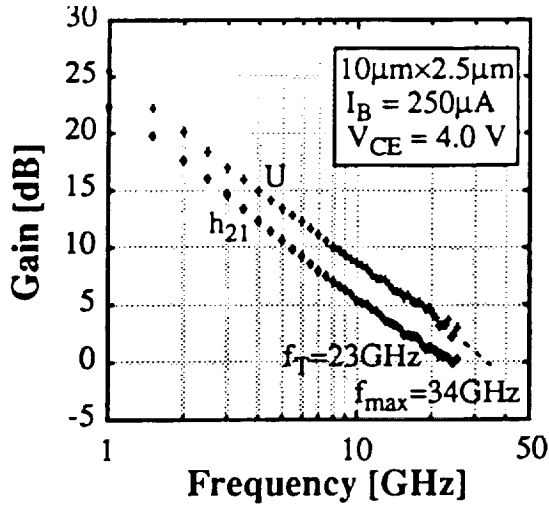


Fig. 2. Frequency response of the fabricated SiGe/Si HBT

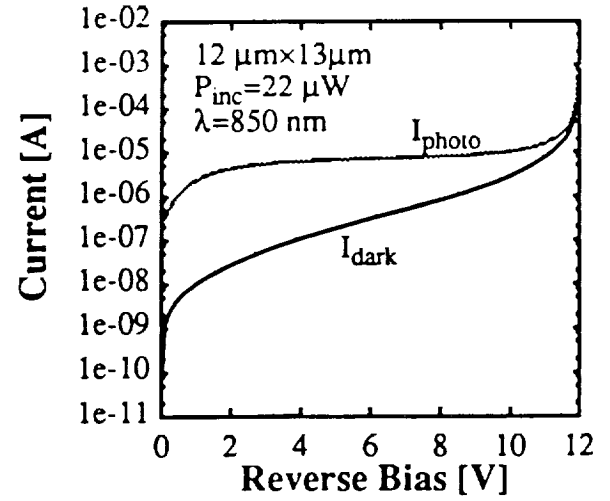


Fig. 3. Dark- and photo-current of the fabricated photodiode

f_{\max} of the device were obtained from the extrapolation of the values of current gain h_{21} and unilateral power gain U at 20 GHz with the assumption of -6 dB/octave roll-off. They are 23 GHz and 34 GHz, respectively, as shown in Fig. 2. The f_{\max} value is believed to be limited by the base resistance, especially base access resistance and base spreading resistance arising from the thin base region (300 Å) and insufficiently high base doping level, which is measured to be $1 \times 10^{19} \text{ cm}^{-3}$ by spreading resistance analysis. With a higher base doping level and the modification of emitter area and shape, enhanced f_{\max} value is expected.

Electrical and optical properties of mesa type PIN photodiodes, employing SiGe p+ base layer and Si n- collector layer of HBTs as p-type contact layer and intrinsic absorption layer, respectively, were characterized. The device has a $12 \mu\text{m} \times 13 \mu\text{m}$ lateral dimension and ring-shaped p-type contact, so that the incident light can be absorbed through the inner square of the ring, while the electric field in the absorption region is kept symmetric for the uniform collection of the generated carriers. Figure 3 shows the dark- and photo-current of a device with the incident light of power $P_{\text{inc}} = 22 \mu\text{W}$ at $\lambda = 850 \text{ nm}$. The dark-current level of the photodiodes were measured to be 100-200 nA at 5 V, which is rather high. The high values are believed to result from the base metal annealing during which base metal possibly penetrates through the thin base layer, leaving the B-C junction leaky. The measured responsivity has a typical value of 0.3 A/W at 5 V and increases steadily as the reverse bias is increased. This responsivity is quite reasonable for optical receiver applications. Corresponding external quantum efficiency is 43%. The bandwidth of the photodiodes was measured with the following measurement setup. Light from a GaAs semiconductor laser with the center frequency of

$\lambda=850$ nm was coupled into a single-mode optical fiber and modulated by an modulator and a HP8350 sweeper. A polarization controller was inserted at the input of the modulator to minimize the coupling loss. The modulated light was focused on photodiodes with a tapered optical probe and the electrical response of devices was measured with a HP8593A spectrum analyzer. An amplifier was inserted at the input of the spectrum analyzer to enhance the power level of the electrical response of photodiodes. The bandwidth of the photodiodes measured were around 450 MHz at the reverse bias of 9 V. It was observed that the bandwidth increases as the applied reverse bias increases. This relatively low bandwidth can be ascribed to the slow diffusion effect of the generated carriers. The intrinsic absorption region of the fabricated photodiodes was proved to be too thin and only a small portion of the incident photons are absorbed in that region. A much more numbers of photons are absorbed and corresponding carriers are generated in subcollector and bulk regions, in which case the photo-generated carriers travel a long distance to reach electrodes by slow diffusion mechanism, resulting in a small bandwidth. By a simple calculation, we can obtain the ratio of photon absorption in the intrinsic region to the total photon absorption. The total photocurrent consists of drift(J_{drift}) and diffusion($J_{diffusion}$) components, which arise from the carrier generation in the depleted region and the neutral region, or intrinsic region and subcollector/bulk region in the given structure, respectively. Each component can be expressed in terms of the device parameters as[8],

$$J_{drift} = -q \int_0^W G(x) dx = q\Phi_0(1 - e^{-\alpha W}) \quad (1)$$

$$J_{diffusion} = q\Phi_0 \frac{\alpha L_p}{1 + \alpha L_p} e^{-\alpha W}, \quad (2)$$

where $G(x)$ is the hole-electron pair generation rate, Φ_0 is the incident photon flux per unit area, α is the absorption coefficient, W is the width of the intrinsic region, and L_p is the hole diffusion length in the bulk region. Therefore, the ratio of the number of the generated of carriers in the intrinsic region to the total number of the generated of carriers, which is identical to the ratio of photon absorption in the intrinsic region to the total photon absorption, can be expressed as,

$$\frac{J_{drift}}{J_{total}} = \frac{J_{drift}}{J_{drift} + J_{diffusion}} = \frac{(1 + \alpha L_p)(1 - e^{-\alpha W})}{(1 + \alpha L_p - e^{-\alpha W})}. \quad (3)$$

By substituting $\alpha=650 \text{ cm}^{-1}$ for Si at $\lambda=850$ nm, $W=250$ nm, $L_p=4.5 \text{ }\mu\text{m}$ in the subcollector, we obtain the value of the ratio to be 0.068. This implies that less than 7% of the total carrier generation occurs in intrinsic region, while more than 93% of the total carrier generation occurs either in subcollector or bulk region in the given photodiode structure. This strongly

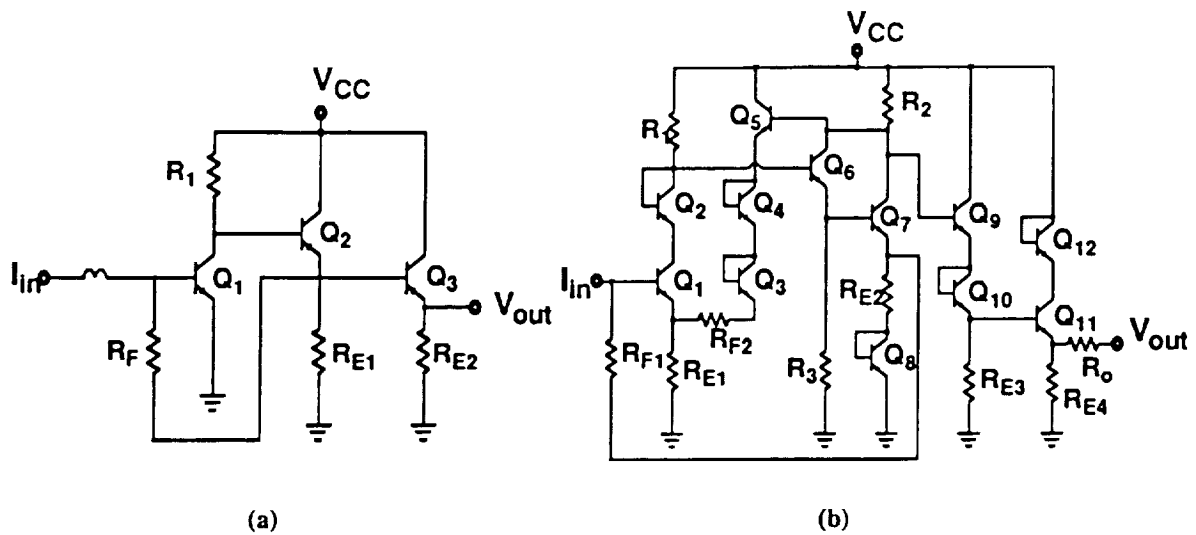


Fig. 4. (a) Circuit diagram of the fabricated single-feedback transimpedance amplifier (b) Circuit diagram of the fabricated dual-feedback transimpedance amplifier

suggests that the bandwidth of the device is dominated by the carriers generated in the subcollector and bulk region which is very slow, and this explains the measured small bandwidth. By increasing the thickness of the intrinsic layer, more portion of the injected photons are expected to be absorbed in the intrinsic layer so that transit time through the depletion layer dominates the speed of the device, leading to the improvement of bandwidth. This is contrary to the common belief that the thinner the intrinsic layer, the larger the bandwidth. Too thick an intrinsic layer, however, will result in the increase of transit time, leading to the degradation of the speed. This implies that there exists an optimum value for the intrinsic layer thickness in terms of the bandwidth of photodiodes.

Single- and dual-feedback transimpedance amplifiers based on SiGe/Si HBTs with emitter size of $5\mu\text{m}\times 5\mu\text{m}$ were designed, fabricated and characterized. Figure 4(a) shows the circuit diagram of the single-feedback transimpedance amplifier. It is composed of a common emitter gain stage, two emitter follower buffers, a resistive feedback loop, and a front-end inductor. The feedback resistor R_F determines the bandwidth, gain, and noise characteristics of the amplifier and the value should be selected based on the trade-off between these parameters. By the increase of R_F value, the gain and noise characteristics of the amplifiers are improved, while the bandwidth is degraded. In this study, the value of R_F was chosen to be $550\ \Omega$, with slightly more emphasis on the bandwidth. The circuit diagram of the dual-feedback amplifier is shown in Fig. 4(b). It includes a second gain stage following the first one, and an extra feedback loop including a resistor R_{F2} . This second feedback, along with the reduced value of

R_{F1} (200 Ω), increases the bandwidth of the amplifier. Second gain stage amplifies the signal to a higher level, compensating for the possible reduction of gain at the first stage from the additional feedback resistance, consequently leading to an increase in overall gain-bandwidth product of the amplifier compared to the single-feedback amplifier. The S-parameters of the fabricated amplifiers were measured with a HP8510 network analyzer in the 0.1 GHz-10.0 GHz frequency range. Figure 5(a) shows the transimpedance gain versus frequency characteristics of a single-feedback amplifier circuit. It shows a transimpedance gain of 45.2 dB Ω and -3 dB bandwidth of 3.2 GHz at the bias point $V_{CC}=3$ V. The frequency response of a dual-feedback amplifier is shown in Fig. 5(b). The transimpedance gain is 47.4 dB Ω and the -3 dB bandwidth is measured to be 3.3 GHz at the bias point of $V_{CC}=7$ V, which shows improvement in both gain and bandwidth compared with the single-feedback version as the design of the circuit intended. Some uncharacteristic ripples are shown in the frequency response of the amplifiers. These are believed to originate from an electrical oscillation generated within the measurement system consisting of the network analyzer and a DC voltage power supply. A moderate gain overshoot can also be seen in the frequency response of the circuits. This is ascribed to the parasitic inductance arising from the narrow coplanar ground line surrounding the whole circuit.

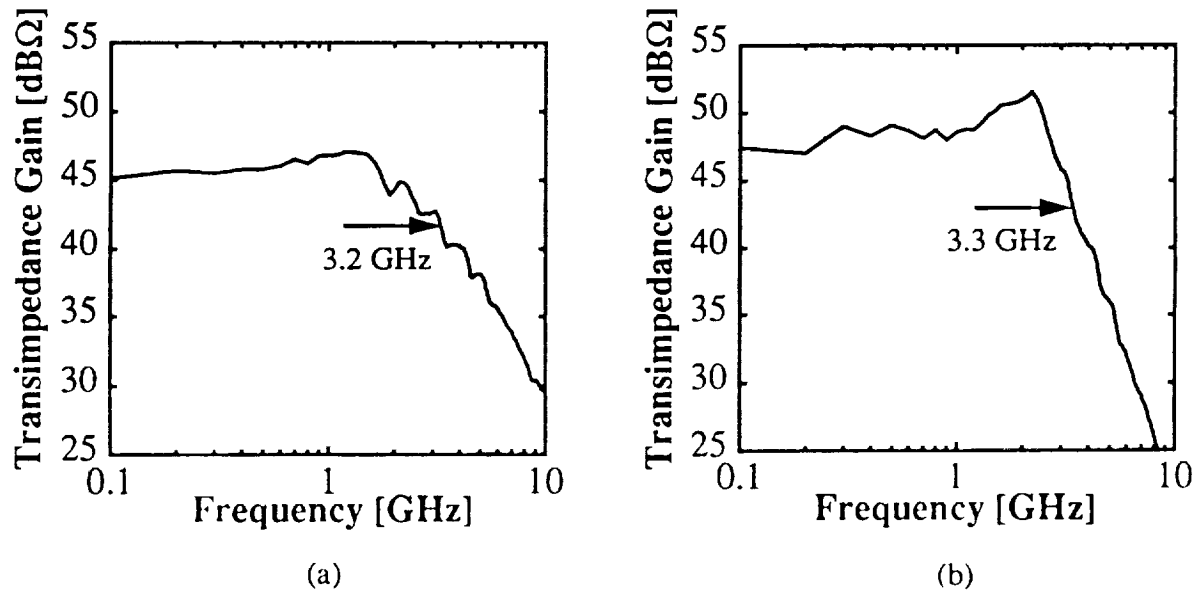


Fig. 5. (a) Frequency response of the fabricated single-feedback transimpedance amplifier
(b) Frequency response of the fabricated dual-feedback transimpedance amplifier

wavelength range of the fabricated photoreceivers will be suitable for optical data link application, which does not require 1.3 μm nor 1.55 μm wavelength for low dispersion and loss. By implementing the collector layer of the SiGe/Si HBT, which is shared as the absorption layer of the photodiode, with SiGe alloys with 20%-40% Ge concentration, the detectable wavelength range of the SiGe photoreceiver will be extended up to 1.3 μm and even to 1.55 μm , and it may find applications even in long-haul optical communication systems. To implement the thick absorption layer with relatively high Ge concentration without significant dislocation, special buffer layers such as graded SiGe buffer layers, superlattice buffer layers, or low temperature Si buffer layers will be required[9].

IV. Conclusion

SiGe/Si PIN-HBT technology has been developed and applied to the fabrication of transimpedance amplifiers and monolithic SiGe/Si photoreceivers for the first time. A SiGe/Si HBT exhibited the f_T and f_{max} of 23 GHz and 34 GHz, respectively, with the DC gain of 25. Mesa-type PIN photodiode showed responsivity of 0.3 A/W at $\lambda=850$ nm and diffusion limited bandwidth of 450 MHz. Fabricated single- and dual-feedback transimpedance amplifiers exhibited the bandwidth of 3.2 GHz and 3.3 GHz with the transimpedance gain of 45.2 dB Ω and 47.4 dB Ω , respectively. Fabricated monolithic photoreceiver showed the bandwidth of 460 MHz, which is apparently limited by the performance of photodiodes. With the optimization of the PIN-HBT material structure, the bandwidth of the photodiode is expected to be improved to exceed that of transimpedance amplifiers. Combined with the design optimization of the transimpedance amplifiers, this will result in monolithic SiGe/Si photoreceivers operating at multi Gb/s for optical communication applications. The application can be extended to long-haul fiber optical communication systems by employing SiGe alloy to the absorption layer of PIN photodiode.

Acknowledgments

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**Monolithically Integrated
SiGe/Si PIN-HBT Front-End Photoreceivers**

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Abstract

Fabrication and characterization of monolithically integrated SiGe/Si PIN-HBT transimpedance photoreceivers are reported. SiGe/Si technology has been developed leading to SiGe/Si HBTs with $f_T = 23$ GHz and $f_{max} = 34$ GHz, and to PIN photodiodes with responsivity of 0.3 A/W at $\lambda = 850$ nm and bandwidth of 450 MHz. SiGe/Si HBT transimpedance amplifiers showed transimpedance gain of 52.2 dB Ω and bandwidth of 1.6 GHz, and the photoreceivers exhibited the bandwidth of 460 MHz.

I. Introduction

The commercial market for optoelectronic integrated circuits (OEICs) is expanding at a rapid rate and the envisaged huge demand for OEICs will necessitate large-scale production of these components, which requires a technology that provides low cost and high reliability as well as high speed operation. Existing Si technology is low cost and provides high reliability. There have been several reports on the implementation of OEICs, especially monolithic photoreceivers, with Si technology[1-4]. SiGe/Si technology is developing rapidly and has been proven to overperform Si technology in terms of the speed of devices[5]. SiGe/Si technology is also expected to provide low cost and high reliability as it is compatible with the well-matured Si technology. There have been reports on photodiodes based on SiGe/Si technology[6-9]. However, no results on monolithically integrated front-end photoreceivers based on SiGe/Si technology have yet been reported. In this study, we report the first monolithically integrated SiGe/Si PIN-HBT front-end photoreceiver circuit based on SiGe/Si HBTs and SiGe/Si photodiodes.

II. Fabrication of Front-End Photoreceiver Circuits

The schematic of the SiGe/Si PIN-HBT structure, grown by one step molecular beam epitaxy (MBE) is shown in Fig 1(a). It is basically a double heterojunction npn HBT structure. The emitter and collector layers consist of Sb-doped Si, while the base layer is a B-doped $\text{Si}_{1-x}\text{Ge}_x$ alloy, which has a smaller bandgap than Si. The Ge mole fraction in the base layer is graded from $x=0.1$ (emitter side) to $x=0.4$ (collector side) to generate a quasi-electric field and to accelerate electrons travelling across the base toward the collector. Spacer layers are inserted on both sides of the base to minimize the effect of dopant outdiffusion during epitaxy, processing, and circuit operation. The base and collector layers of the HBT are used to form the PIN photodiode. Note

that the absorption layer of the photodiode is Si. This kind of one step epitaxy approach provides advantages over regrowth such as better planarity, simpler processing, and higher yield. The epitaxial layers were grown at the rate of 2 Å/sec at a background pressure of 6×10^{-9} Torr. The growth temperature was 415 °C for the collector and emitter layers, and 550 °C for the base layer.

Monolithically integrated SiGe/Si PIN-HBT photoreceivers based on the SiGe/Si HBTs with an emitter size $A_E = 5 \times 5 \mu\text{m}^2$ and the photodiodes with a mesa size of $A_M = 12 \times 13 \mu\text{m}^2$ have been designed for fabrication and characterization. Figure 1(b) shows the circuit diagram of the photoreceiver with a transimpedance amplifier. It consists of a photodiode, common emitter gain stage, two emitter follower buffers, and a resistive feedback loop. Q_1 , Q_4 , and Q_5 are inserted as level shifting diodes. Two voltage sources, V_{DD} and V_{CC} , are used for diode and circuit biasing, respectively, to optimize the operating points independently. The value of the feedback resistor R_F determines the bandwidth, gain, and noise characteristics of the photoreceiver and should be chosen based on a trade-off between these parameters. In this circuit, the value of the feedback resistor R_F was chosen to be 640 Ω. The fabrication procedure for the photoreceiver circuits is as follows. The emitter contact (Cr/Au=500/2000 Å) is defined by evaporation, followed by emitter mesa formation with a combination of SF_6 and O_2 -based dry etching and KOH-based wet etching. This two step etch provides minimal emitter undercut and base overetch, resulting in the reduction of base access resistance. Evaporation of the self-aligned base metal (Pt/Au=200/1300 Å), which is also used as the p-contact for PIN photodiodes, follows and then the base mesa is formed by dry etching. Collector contact (Ti/Au=500/2000 Å) is defined by evaporation on the exposed highly doped subcollector layer, which is also shared as an n-contact for photodiodes. Device isolation by dry etching is followed by SiO_2 layer deposition with plasma-enhanced chem-

ical vapor deposition (PECVD) and via hole formation. Thin film resistor(NiCr=700 Å) and inter-connection metal(Ti/Al/Ti/Au=500/11000/500/3000 Å) layers are subsequently evaporated. Finally, airbridges are built up by the evaporation of thick metal(Ti/Al/Ti/Au=500/16000/500/3000 Å). The schematic cross section profile of the fabricated circuit is shown in Fig. 2.

III. Results and Discussion

Device characteristics of npn SiGe/Si HBTs, fabricated with the processing procedure above, have been obtained with DC and RF measurements. The DC current gain β was measured to be 25, while collector and base ideality factors were extracted to be $n_c=1.12$ and $n_b=1.84$, for the device with an emitter size of $A_E=2.5 \times 10 \mu\text{m}^2$. The current-voltage characteristics of the device are shown in Fig 3(a). The frequency response was obtained from the S-parameters measured with a HP8510 network analyzer in the 0.5-25.5 GHz frequency range. Values for cut-off frequency f_T and maximum oscillation frequency f_{max} of the device are 23 GHz and 34 GHz, respectively. The device with an emitter size of $A_E=5 \times 5 \mu\text{m}^2$, which has been incorporated into the circuits, exhibits f_T and f_{max} of 25 GHz and 21 GHz, respectively.

Electrical and optical properties of mesa type PIN photodiodes, fabricated from the HBT samples, were also measured. The device area is $12 \times 13 \mu\text{m}^2$ and a ring-shaped metal contact is formed on the top p^+ SiGe layer. To enhance the optical coupling efficiency, a PECVD SiO_2 layer of $1.1 \mu\text{m}$ thickness was deposited as an antireflection coating. The dark current and photocurrent of the photodiode with $22 \mu\text{W}$ incident optical power at $\lambda=850 \text{ nm}$ are shown in the inset to Fig. 3(b). The measured responsivity was 0.3 A/W at a reverse bias of 5 V and steadily increased as the reverse bias was increased. The corresponding external quantum efficiency is 43%. The band-

width of the photodiode measured with $\lambda=850$ nm light was an increasing function of the reverse bias and was around 450 MHz at a reverse bias of 9 V, as shown in Fig. 3(b). This rather small bandwidth can be ascribed to the slow diffusion and the recombination of carriers generated outside the absorption layer. The n^- absorption layer of the photodiode is relatively thin (2000 Å) and very small fraction of the incident photons are absorbed in this region, compared to those absorbed outside it. Our calculations indicate that the diffusion current constitutes more than 90% of the total photocurrent for the given photodiode structure. This performance can be compared to those of waveguide PIN photodiodes, where incident photons are absorbed mostly in the waveguide absorption region owing to the difference in the refractive index of Si and SiGe alloy, exhibiting GHz-ranged bandwidths[6-9].

The electrical characteristics of the transimpedance amplifier were measured with a HP8510 network analyzer. The transimpedance gain of the amplifier is 52.2 dBΩ and the bandwidth is 1.6 GHz. The frequency response of the photoreceiver circuit was measured with the system used for the photodiodes. Figure 3(c) shows the relative frequency response of the fabricated photoreceiver excited with $\lambda=850$ nm light at the biases $V_{DD}=9$ V and $V_{CC}=6$ V. The -3 dB bandwidth was measured to be 460 MHz, which is close to the bandwidth of the photodiode and far smaller than that of the transimpedance amplifier. This strongly implies that the bandwidth of the photoreceiver is limited by that of the photodiode, not by the bandwidth of the transimpedance amplifier. The bandwidth of the photoreceiver is expected to increase by optimizing the photodiode structure. Since direct sensitivity measurements could not be made, the noise characteristics of the photoreceiver were calculated with a noise equivalent circuit, taking into account the photodiode dark-current shot noise, base- and collector-current shot noise, and thermal noise generated by the feedback resistor and the biasing resistor of the first gain stage. The calculated input noise

current spectral density is $8.2 \text{ pA}/\sqrt{\text{Hz}}$ up to 1 GHz, dominated by shot noise from base current and thermal noise from the feedback resistor. With this value of noise current, estimated photoreceiver sensitivities of -24.3 dBm and -22.8 dBm are obtained for 0.5 Gb/s and 1 Gb/s, respectively, for a bit-error rate (BER) of 10^{-9} and $\lambda=850 \text{ nm}$.

IV. Conclusion

SiGe/Si PIN-HBT technology has been developed and applied to the fabrication of monolithically integrated SiGe/Si photoreceivers. The HBTs exhibit f_T and f_{max} of 23 GHz and 34 GHz, respectively. Mesa-type PIN photodiodes showed responsivity of 0.3 A/W at $\lambda=850 \text{ nm}$ and a diffusion limited bandwidth of 450 MHz. The SiGe/Si HBT transimpedance amplifiers have a transimpedance gain of 52.2 dB Ω and bandwidth of 1.6 GHz. The optical bandwidth of the SiGe/Si photoreceivers was measured to be 460 MHz, which is apparently limited by that of the photodiodes. The sensitivity values of the photoreceiver are calculated to be -24.3 dBm and -22.8 dBm for 0.5 Gb/s and 1 Gb/s, respectively, for BER of 10^{-9} and $\lambda=850 \text{ nm}$.

Acknowledgment

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Figure Captions

Figure 1. (a) SiGe/Si HBT grown by molecular beam epitaxy; (b) Circuit diagram of the photoreceiver.

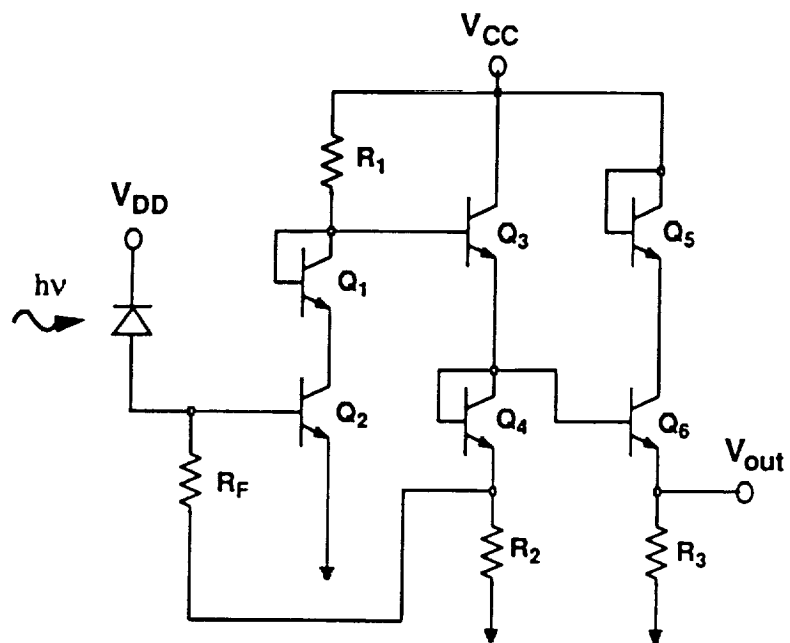
Figure 2. Schematic cross section profile of the fabricated photoreceiver.

Figure 3. (a) Measured current-voltage characteristics of the HBT; (b) Measured frequency response of the photodiode with the dark- and photocurrent variation shown in the inset. The solid line shows the fits to the measured response; (c) Measured frequency response of the photoreceiver. The solid line shows the fits to the measured response.

Emitter Contact	Si	n⁺	1×10¹⁹	200 nm
Emitter	Si	n	2×10¹⁸	100 nm
Spacer	Si_{0.9}Ge_{0.1}	i		1 nm
Base	Si_{1-x}Ge_x x:0.1→0.4	p⁺	5×10¹⁹	30 nm
Spacer	Si_{0.6}Ge_{0.4}	i		10 nm
Collector	Si	n⁻	1×10¹⁶	250 nm
Subcollector	Si	n⁺	1×10¹⁹	1.5 μm
Substrate	Si	p⁻	2×10¹²	540 μm

(a)

Figure 1



(b)

Figure 1

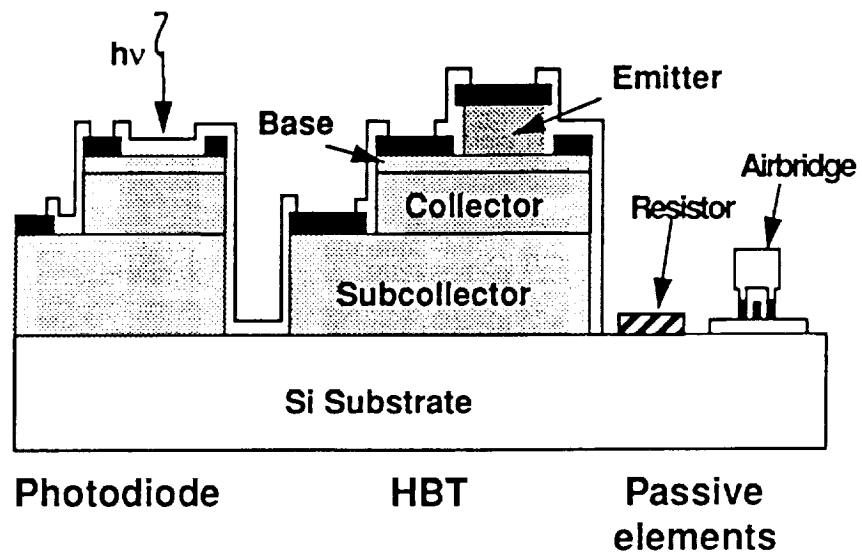
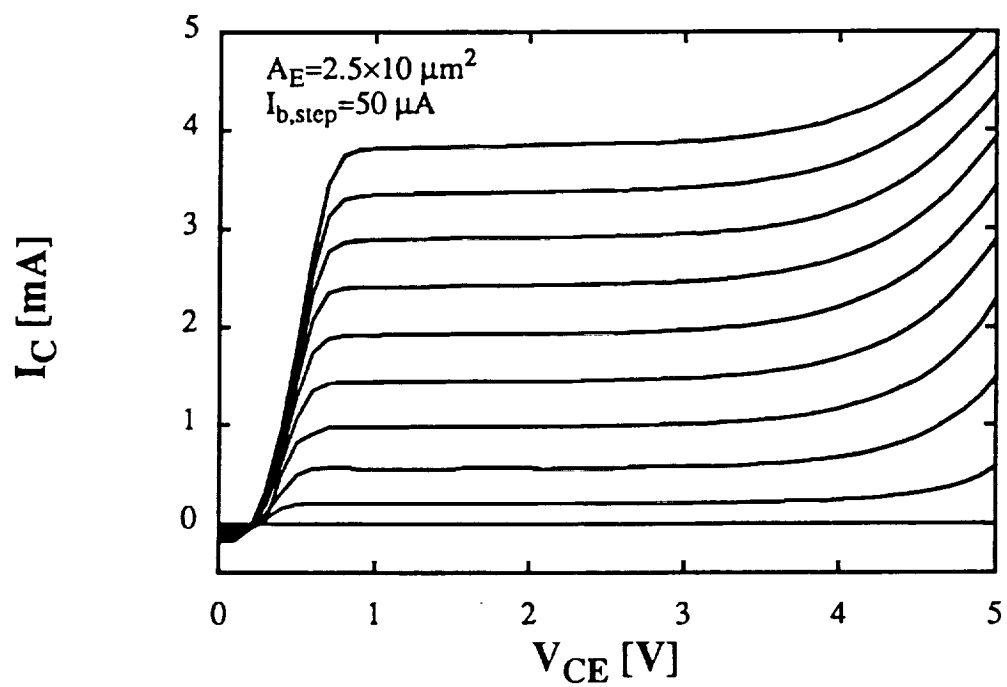
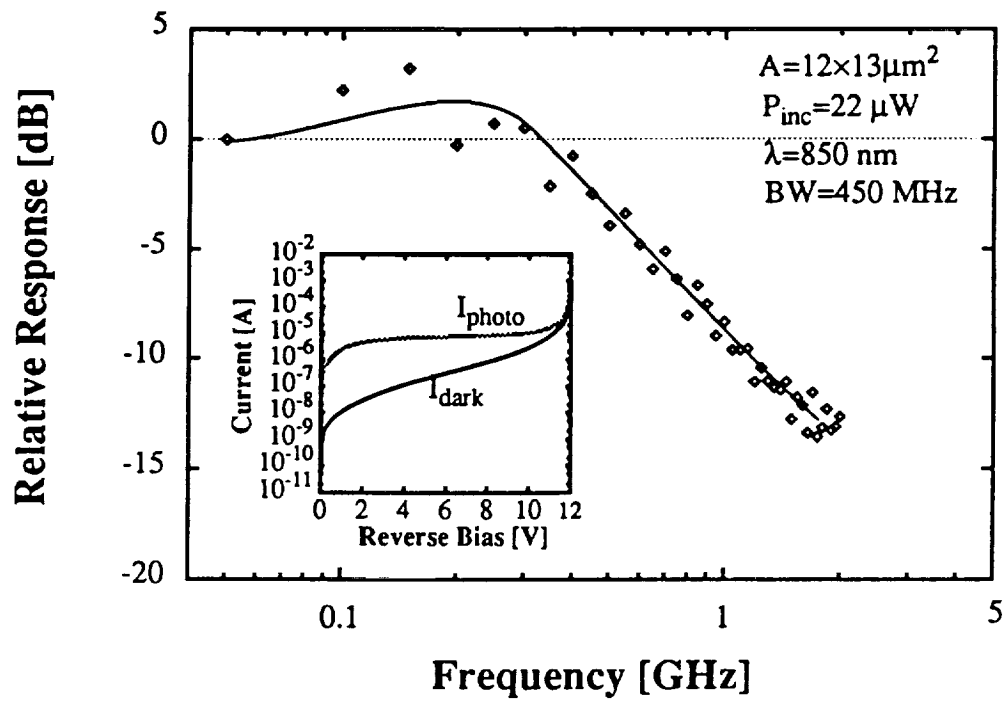


Figure 2



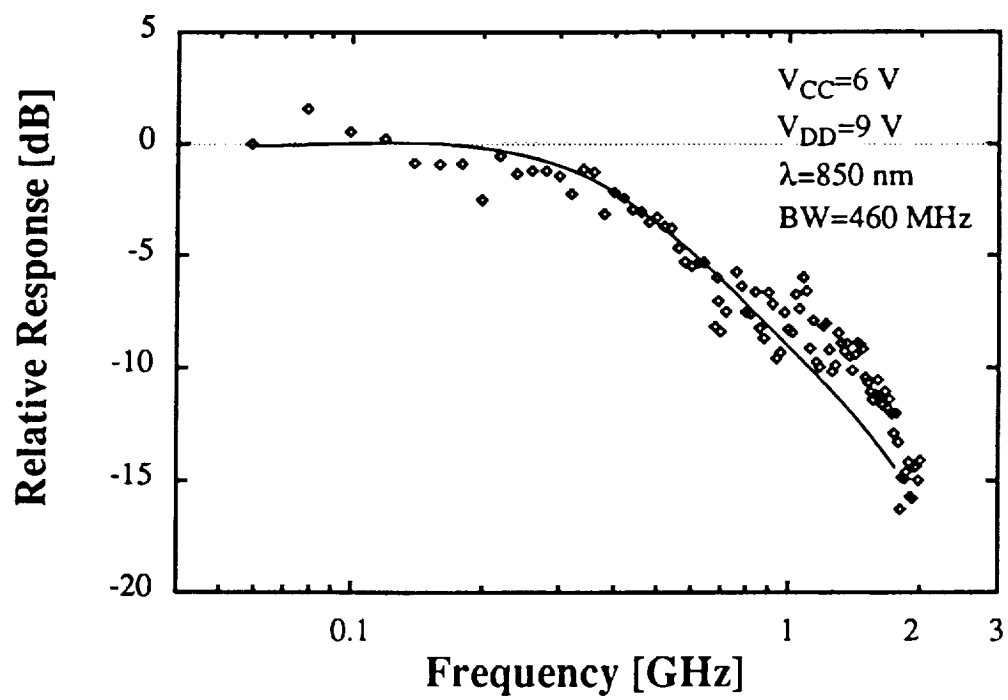
(a)

Figure 3



(b)

Figure 3



(c)

Figure 3

X- and Ku-band Amplifiers Based on Si/SiGe HBTs and Micromachined Lumped Components

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Abstract

Double mesa structure Si/SiGe heterojunction bipolar transistor(HBT) and novel micromachined lumped passive components have been developed and successfully applied to the fabrication of X-band and Ku-band monolithic amplifiers. The fabricated $5 \times 5 \mu\text{m}^2$ emitter size Si/SiGe HBT exhibited a DC current gain β of 109, and f_T and f_{max} of 28 GHz and 52 GHz, respectively. Micro-machined spiral inductors demonstrated resonance frequency of 20 GHz up to 4 nH, which is higher than that of conventional spiral inductors by a factor of 2. Single-, dual-, and three-stage X-

band amplifiers have been designed, based on the extracted active and passive device model parameters. A single-stage amplifier exhibited a peak gain of 4.0 dB at 10.0 GHz, while dual- and three-stage versions showed peak gains of 5.7 dB at 10.0 GHz and 12.6 dB at 11.1 GHz, respectively. A Ku-band single-stage amplifier has also been designed and fabricated, showing a peak gain of 1.4 dB at 16.6 GHz. Matching circuits for all these amplifiers were implemented by lumped components, leading to a much smaller chip size compared to those employing distributed components as matching elements.

I. Introduction

As the major application field of microwave circuits shifts from military to commercial markets, monolithic microwave integrated circuits (MMICs) based on Si technology have received great attention due to their lower cost compared to III-V components. Also attractive as the main advantages of Si MMICs are the matured Si technology, compatibility with Si CMOS technology, mechanical stability of Si substrate, and superior thermal conductivity of Si. In particular, CMOS compatibility opens a great opportunity for the integration of radio frequency (RF) modules into low frequency circuitry. In view of these facts, a great expansion of the Si MMIC market is anticipated in the near future.

The first attempt to fabricate Si based microwave circuits can be traced back to the 1960's[1]. Since then, however, the development of Si monolithic microwave circuits has been impeded by several obstacles, the most significant of which are the absence of semi-insulating substrate and the inferior operation frequency of Si based devices. Recently, these two shortcomings have been removed by the availability of high-resistivity Si substrate and the emergence of high quality SiGe epitaxial layers. It has been reported that the dominant factor in transmission line loss is conductor loss, rather than dielectric loss, if the resistivity of the substrate is close to or higher than $10 \text{ k}\Omega\text{cm}$ [2]. Fortunately, the matured impurity control techniques at the present time have led to the production of Si substrate with $\rho > 10 \text{ k}\Omega\text{cm}$, so that the lossy substrate may not be a limitation for Si MMICs. On the other hand, the recent advances in the growth of epitaxial SiGe layers have led to high quality Si/SiGe heterojunctions and, consequently, to high performance Si based devices employing these heterojunctions. This development of Si/SiGe device technology, especially that of Si/SiGe HBTs, has pushed the operating frequency of these devices to higher

than 100 GHz, approaching that of GaAs based devices and eliminating the remaining limitation for Si MMICs[3-5].

Owing to the breakthrough in the Si based device technology, there have been a number of reports on successful implementation of Si/SiGe HBT based MMICs operating at X-band or at even higher bands. Voltage controlled oscillators(VCOs) with oscillation frequency of 26 GHz and 40 GHz[6] and X-band mixers[7] have been realized based on Si/SiGe HBTs. A narrow band amplifier at Ka-band[8] and a wideband amplifier up to Ku-band[9] have also been implemented with Si/SiGe HBTs. However, all these circuits are designed with distributed matching components, resulting in rather large circuit areas. For large scale integration of circuits, which is essential in future commercial applications, reduction of chip size is critical. This can be achieved by employing lumped components as matching elements, owing to their smaller dimensions compared with distributed ones up to 30 GHz. Lumped components, however, generally suffer from low resonance frequency and this limits the frequency range of lumped matching circuits. This strongly motivates the development of lumped components with higher resonance frequency, compatible with Si based microwave transistors. In this study, novel micromachined lumped passive components on Si substrate have been developed, leading to a drastic improvement in the resonance frequency of inductors. Based on this, a Si/SiGe MMIC technology, combining double mesa structure Si/SiGe HBT technology and the micromachining technique has been developed. With this technology, X- and Ku-band Si/SiGe monolithic circuits employing micromachined lumped component matching networks have been successfully implemented for the first time.

In this paper, the details of the Si/SiGe HBT MMIC technology are described in section II, followed by section III describing the performances of active and passive devices. The design and performance of single-, dual- and three-stage X-band amplifiers and a single-stage Ku-band

amplifier is described and discussed in section IV. Conclusions are made in section V.

II. Technology

Growth of high-quality epitaxial layers and reproducible and reliable processing are the key factors in the successful development of high performance devices and circuits. We have grown npn double heterojunction Si/SiGe HBT structures and developed a stable SiGe MMIC process. Two methods are widely used for the growth of Si/SiGe heterostructures: MBE growth and UHV/CVD growth. MBE growth benefits from the larger dynamic range in doping concentration (10^{14} – 10^{21} cm⁻³) and lower growth temperature, while UHV/CVD growth offers higher throughput, which is favored for mass production[10]. In this study, the HBT heterostructures were grown by MBE, except for the thick subcollector layer(Fig. 1). The detailed growth sequence is as follows: arsenic-doped subcollector layer(1.5 μ m) is grown by CVD on a high-resistivity (100) Si wafer, whose resistivity is higher than 10k Ω cm according to a spread resistance analysis(SRA). Then, the wafer is loaded into the MBE chamber for the growth of antimony-doped Si collector layer and boron-doped SiGe base layer. Two design issues for base layer are briefly discussed here: spacer layers and Ge composition profiles. The outdiffusion of boron, which may occur during the epitaxy, processing, and circuit operation, is known to move the p-n junction toward the emitter, away from the Si/SiGe heterojunction. This would give rise to parasitic energy barriers in the conduction band, resulting in the increase of the base transit time τ_B and the reduction of the cutoff frequency f_T [11]. To suppress the boron outdiffusion, intrinsic spacers are frequently introduced as a buffering layer. In this study, a 50 Å spacer layer is inserted on both sides of the base layer and no significant outdiffusion effects have been observed. A uni-

form Ge composition profile of 40% is employed for the SiGe alloy in the base layer. Compared with a graded composition profile (smallest mole fraction at E-B junction), uniform profile shows larger base transit time τ_B due to the absence of the quasi-electric field. But, the larger bandgap offset at the E-B junction in the case of a uniform profile provides larger current gain β and smaller emitter delay time τ_E [12]. In addition, the larger Ge composition at E-B junction reduces the possibility of overetching the base layer during the selective wet etching of emitter layer in mesa type HBT processing, since the selectivity is higher for larger Ge composition in SiGe alloy. This leads to a smaller base access resistance. The Ge composition profile is determined by a trade-off between these parameters and the uniform profile was favored in this study. Base doping concentration is another issue in base design. SRA result shows that the base doping concentration of the structure is $2 \times 10^{19} \text{ cm}^{-3}$, which is believed to be underestimated because the measurement step is about the same order as the base layer thickness. The actual concentration is believed to be close to $1 \times 10^{20} \text{ cm}^{-3}$, including unactivated dopants, which are not considered in SRA. After the growth of the base layer and spacer layers, antimony-doped Si emitter layer and emitter cap layer are deposited subsequently. All the MBE epitaxial layers were grown at a rate of 2 Å/min at a background pressure of $6 \times 10^{-9} \text{ Torr}$. The growth temperature was 550 °C for the base layer and 415 °C for the collector and emitter layers.

SiGe MMICs with double mesa structure HBTs have been fabricated with standard lift-off and etching techniques, using the epitaxial wafers described above. The process starts with emitter metal contact formation (Cr/Au = $500/2000 \text{ Å}$) on the highly-doped emitter contact layer by evaporation and lift-off. The metal contact is used as an etch mask for the following base layer exposure step. The base exposure is the most critical step in the fabrication of mesa-type HBTs since this process directly affects the f_{max} of the devices through the parasitic base resistance R_B .

Hence, this step is discussed here in more detail. Overetching of the base layer and the excessive lateral undercut of emitter sidewall should be avoided to keep the value of R_B small, while moderate undercut and vertical emitter sidewall profile are required for the following self-aligned base metal deposition. To meet these requirements, we have employed an angled emitter contact formation and two step etching. Two step etching is performed by the combination of dry and wet etching. First, SF_6 and O_2 -based anisotropic reactive ion etch (RIE) removes the biggest portion of the emitter layer without undercut. Second, KOH-based selective solution ($\text{KOH}:\text{K}_2\text{Cr}_2\text{O}_7:\text{H}_2\text{O}=50\text{g}:2\text{g}:200\text{ml}$) etches away the remaining emitter layer and stops close to the E-B heterojunction. The etching selectivity of the KOH solution was found to be higher than 10 at 30 °C for Ge composition of 40%. With this two step etching, emitter sidewall undercut can be much reduced since the sidewall is laterally etched only during the short wet etching cycle. The purpose of the angled emitter contact pattern is as follows. The etch rate of the Si in KOH-based solution is crystal-orientation dependent, exhibiting much smaller etch rate for (111) orientation compared with those for (100) and (110) orientations[13][14]. This orientation dependence gives rise to trapezoidal sidewall etch profile when etch mask patterns on (100) wafers are aligned along (110) orientation, which is parallel to the major flat of the wafer. On the other hand, vertical sidewall profile can be obtained when the etch mask patterns are aligned along (100) orientation, which is 45° off the major flat of (100) wafer. This is depicted in Fig. 2 with SEM pictures, which show resultant trapezoidal and vertical sidewall profiles for etch mask patterns aligned along (110) orientation(A-B), and (100) orientation(C-D), respectively. Therefore, the self-aligned deposition of base metal, using emitter metal patterns as etch mask for KOH-etching, will be successful only if emitter patterns are aligned 45° off the major flat. Otherwise, the base metal will eventually touch the protruding emitter sidewall, electrically shorting the emitter and base. Rapid thermal anneal-

ing(RTA) is done for 20 sec at 400 °C for the optimized ohmic contact of emitter metal. After the self-aligned base metal deposition(Pt/Au=200/1300 Å) by evaporation, the base mesa is formed by RIE, exposing the highly doped subcollector layer for collector contact. Collector metal(Ti/Au=500/2000 Å) contact is defined by evaporation and lift-off, followed by another RTA (3sec, 375 C) for the base and collector ohmic contact. Device isolation RIE finishes the processing steps for active devices, leaving the high-resistivity Si substrate exposed. Passive devices are built on the exposed substrate. Three successive evaporations provide basic building blocks for MIM capacitors; bottom metal layer(Ti/Al/Ti/Au/Ti/Ni=500/9000/500/3000/500/1500Å), dielectric layer(SiO₂=2000Å), and top metal layer(Ti/Ni=500/1000). The bottom metal layer also serves as a feeding line for spiral inductors. Intermetal dielectric layer(SiO₂=1µm), which also passivates HBTs, is deposited by plasma-enhanced CVD(PECVD). On top of the deposited SiO₂ layer, thin film resistor is formed by the evaporation of 500 Å NiCr layer. Via holes for contacts are opened by selective dry etching of the SiO₂ layer. This is followed by a thick metal(Ti/Al/Ti/Au/Al/Ni=500/15000/500/4000/500/1500 Å) evaporation, which provides device interconnection, probing pads, inductor spirals, and top contact of MIM capacitors. Finally, a two step deep RIE removes the exposed SiO₂ layer and Si substrate while active devices and resistors are covered with photoresist for protection. This is the micromachining step which improves the resonance frequency of inductors, as will be discussed in more detail in the next section. No airbridge is employed in this process.

III. Device performance

A. Active devices - Si/SiGe HBTs

Double mesa structure Si/SiGe HBTs with various dimensions have been fabricated and their DC and RF properties were measured. The following discussion will focus on the characteristics of devices with emitter area $A_E=5 \times 5 \mu\text{m}^2$, since these devices have been employed to the design of actual circuits. The devices have base-collector junction area of $A_{BC}=12 \times 13 \mu\text{m}^2$, which is also an important parameter for maximum oscillation frequency f_{max} . The common emitter current-voltage characteristics are shown in Fig. 3(a). As can be seen from the plot, the device suffers from the Kirk effect, which arises from the concentration inversion of injected carriers and space charge in the collector depletion region. This can be ascribed to the relatively low collector doping concentration ($5 \times 10^{15} \text{cm}^{-3}$) of the device. This effect appears to be more severe for low V_{CE} , since the velocity of the injected carriers is smaller at lower voltage leading to the higher effective carrier concentration. However, the device and circuit operation would not be affected by the Kirk effect, provided the operating bias point is chosen outside the value for which the Kirk-effect is operative, and the signal amplitude is not significantly large. The offset voltage of the device is very close to zero, implying the symmetry of E-B and B-C heterojunctions as a consequence of uniform Ge composition across the base layer. Figure 3(b) shows the Gummel plot of the identical device. The collector and base ideality factors are extracted to be $n_c=1.04$ and $n_b=1.79$, respectively. The DC current gain β is measured at the fixed collector-emitter voltage $V_{CE}=4 \text{ V}$, as shown in the inset. Values higher than 100 are obtained for most of the operating current range with the maximum value of 109 occurring at $I_C=10.4 \text{ mA}$. S-parameters have been

measured for a frequency range of 0.5-25.5 GHz with H8510B network analyzer in order to investigate the RF characteristics of the device. Figure 3(c) shows the current gain H_{21} and the unilateral power gain U as a function of the frequency at a bias point of $I_C=7.0$ mA and $V_{CE}=4.0$ V. The corresponding f_T and f_{max} , obtained from the extrapolation of $|H_{21}|$ and U on the assumption of -6 dB/octave roll-off, are 28 GHz and 52 GHz, respectively. Higher f_{max} values could be obtained if the lateral dimension of the device is optimized for smaller base spreading resistance. Measured S-parameters have been utilized for the small signal modeling of the device with a HBT T-model. The equivalent circuit is given in Fig. 4, along with the corresponding parameters extracted from the method proposed in [15].

B. Micromachined passive components

Planar lumped inductors are widely used in MMIC as matching elements, bias chokes and filter components. Compared with distributed transmission line components, lumped components are smaller, especially at frequencies below 30 GHz. As a result, lumped component circuits can be more compact than distributed ones in MMIC applications. However, planar lumped components suffer from parasitic effects. In particular, planar lumped spiral inductors exhibit very low resonance frequencies due to the parasitic capacitance, thus limiting operating frequencies. Work has been done by fabricating the inductors on a dielectric membrane to increase the resonance frequency[16][17]. This technique is difficult to adopt for integration with active devices, since it requires the development of a dielectric membrane between the bulk high-resistivity Si and the doped layers. Recently, an air-gap stacked spiral inductors, using air-bridge technology has been introduced[18]. By stacking metal lines, inductor area can be reduced by 25% to 45% and the resonance frequencies can be increased by 10% to 15% compared with conventional spiral inductors.

However, the increase of resonance frequencies is not enough for MMIC applications in Ku-band or higher.

To obtain a inductor with higher resonance frequency, a new micromachined spiral inductor has been developed, as shown in Fig. 5(a). In this inductor structure, bottom metal layer and interconnection metal layer, separated by a intermetal PECVD SiO₂ layer, form the feed line and spirals of inductors, respectively. By covering the metal structure with Ni which is used as a self-aligned mask and removing the exposed PECVD SiO₂ layer and Si substrate material in between the turns by RIE, the effective dielectric constant of this structure can be reduced. This results in a smaller series and shunt parasitic capacitance from turn to turn (C_C) and from the signal line to ground (C_p) as shown in the equivalent model of the inductor (Fig. 5(b)). Due to the significant reduction of the parasitics, the resonance frequency can be increased drastically. By measuring the dual-port S-parameters of the inductors up to 40 GHz using HP8510C, the resonance frequencies are extracted. Figure 5(c) shows the resonance frequencies of the micromachined inductors and conventional ones. Compared with conventional spiral inductors, a 50% improvement in resonance frequencies can be obtained by a 10 μm -deep RIE, and the improvement can be as high as 100% if a 20 μm -deep RIE is used.

MIM capacitors have been fabricated and characterized. As mentioned earlier, evaporated SiO film($d=2000 \text{ \AA}$) is used as a dielectric material and sandwiched by bottom and top metal layers. Top metal layer protects the dielectric film during via hole opening process and the top feeding contact is provided by much thicker interconnection metal to reduce the parasitic resistance and inductance. SiO is preferred to SiO₂ as a dielectric film, since SiO provides higher dielectric constant, leading to smaller capacitor area. The dielectric constant ϵ_r of the evaporated SiO, extracted from the capacitance and the area of fabricated capacitors, is 4.7, which provides a

capacitance of $0.21 \text{ fF}/\mu\text{m}^2$. The measured capacitors exhibit resonance frequencies higher than 20 GHz up to 1 pF. Since the capacitance values of the matching capacitors in X- and K-band application rarely exceed 1 pF, these capacitors can safely be applied to circuits at these bands.

Thin film resistors are also indispensable components in most microwave circuits, frequently applied to bias circuits and feedback loops. 500 Å NiCr film was evaporated to realize thin film resistors. The sheet resistance of the film is found to be in the range of $45\text{-}50\Omega/\square$.

Interconnection line sections were also fabricated and characterized, since they are frequently employed to connect adjacent components on circuits. They can be considered as electrical shorts in low frequency operations, but they behave mainly as inductors in the microwave frequency range, and their effect have to be considered for rigorous microwave circuit designs. The inductance of line sections shows fairly linear relation with the length of the line, which implies that the total inductance is dominated by self-inductance rather than mutual inductance. The inductance per unit length of 2.2 μm thick, 10 μm wide line sections is found to be around 1.1 pH/ μm . Interconnection line sections may be inserted to circuits on purpose for a fine tuning of inductance matching of circuits.

The test structures for all these passive components were fabricated with various dimensions, which cover the entire range of practical interest. S-parameters were measured for the fabricated test patterns and used for modeling with appropriate equivalent circuits which include possible parasitics as shown in Fig. 5(a) and Fig. 6. This completes a passive components library to be used for circuit design.

IV. Amplifier Design and Performance

After fabrication and characterization of active devices and passive components, the measured S-parameters and equivalent circuit parameters are utilized for circuit design. In this study, X-band single-stage, dual-stage, and three-stage Si/SiGe HBT amplifiers have been designed, fabricated, and characterized. A preliminary result of a Ku-band single-stage amplifier is also discussed.

A. Single-stage amplifier

Figure 7(a) shows the circuit diagram of the X-band single-stage amplifier. Basically, it consists of one Si/SiGe HBT common emitter amplifying stage, along with input and output matching networks and bias circuit. L_1 and C_1 provide a conjugate power matching to the input of amplifying stage, while L_2 and C_2 are employed for output power matching. L_2 also functions as a RF choke. This, together with the bypass capacitor C_3 , isolates V_{CC} from the amplifier. Base current is supplied from the input of the circuit, together with input RF signal.

The photomicrograph of the fabricated circuit is shown in Fig. 7(b). The chip size is $0.75 \times 0.65 \text{ mm}^2$. Considering that circuits with distributed matching components usually stretch up to around half the wavelength at the operating frequency, this chip size may be less than 20% of the corresponding distributed matching circuit. The S-parameters of the fabricated circuit was measured with HP8510C network analyzer with DC bias supplies from HP4145B semiconductor parameter analyzer. The measured transducer gain S_{21} is shown in Fig. 7(c), along with input and output return losses S_{11} and S_{22} at the bias of $V_{CE}=4.7 \text{ V}$ and $I_C=9.9 \text{ mA}$. The bias was optimized for maximum gain. A peak gain of 4.0 dB occurs at 10.0 GHz. The output return loss S_{22} has min-

imum value less than -20 dB, which is reasonably low. However, the minimum value of input return loss S_{11} is only around -7 dB. This may be explained by the process variations which would change parasitic values of devices, thus leading to shifts in S-parameters. Input and output voltage standing wave ratios(VSWR), calculated from the input and output return losses, exhibit minimum values of 2.73 and 1.21, respectively.

A Ku-band single-stage amplifier is also designed and fabricated. The circuit configuration is basically same as X-band version. Only the passive component values are changed to meet the new matching condition at Ku-band. The complete circuit occupies an area of $0.62 \times 0.64 \text{ mm}^2$, which is slightly smaller than X-band circuit, due to smaller passive element dimensions required for higher frequency. The horizontal dimension of the circuit is still less than single-eighth of the wavelength, suggesting that the advantage of lumped matching is still obvious for Ku-band in terms of circuit area. The gain and return losses are shown in Fig 8(a). The gain S_{21} exhibits a peak value of 1.4 dB at a frequency of 16.6 GHz and the gain keeps positive values over 20 GHz, reaching K band. The input return loss S_{22} is close to -25 dB and the output return loss S_{11} exceeds -11 dB. The input and output VSWR of the amplifier have the minimum values of 1.69 and 1.14, respectively, as shown in Fig. 8(b).

B. Dual-stage amplifier

A dual-stage amplifier is designed with a similar approach as the single-stage amplifier and its schematic is shown in Fig. 9(a). It consists of two common emitter stages and three matching networks. Input matching keeps the same configuration as single-stage amplifier consisting of L_1 and C_1 . L_2 and C_2 , L_3 and C_3 constitute interstage and output matching network, respectively. C_2 also functions as a blocking capacitor separating the first and second amplifying stages DC-

wise, and L_2 behaves as RF choke as in the case of the single-stage amplifier. V_{CC} supplies collector voltage for the first stage and, simultaneously, base current for the second stage via a resistor voltage divider. R_1 and R_2 values were carefully selected to give an accurate base-emitter voltage for optimum bias since the base current is very sensitive to the voltage across base and emitter. The resistor values are liable to change from process to process since the film is too thin (500 Å) to be accurately controlled by evaporation. However, the ratio of R_1 and R_2 is unchanged, even if the absolute resistance values fluctuate, leading to a stable base current supply at the input of the second stage. The base current for the first stage and the collector voltage for the second stage are supplied through the input and output port of the amplifier, respectively. The photomicrograph of the fabricated circuit is shown in Fig. 9(b). The chip size is $0.98 \times 0.80 \text{ mm}^2$, which is 60% larger than that for the single-stage amplifier. In this context, it is apparent that the area per stage reduces as the number of stage increases. The gain is 5.7 dB at 10.0 GHz and the input and output return loss remains between -5 dB and -10 dB (Fig. 9(c)). The higher complexity of the circuit, compared with single-stage amplifier, is believed to result in poor return loss and lower gain per stage.

C. Three-stage amplifier

A three-stage amplifier is designed in a manner similar to the single- and dual-stage amplifiers. Three common emitter amplifying stages and 4 matching networks are the basic building blocks for the amplifier (Fig. 10(a)). Similar to the dual-stage amplifier case, V_{CC1} supplies collector voltage to the first stage and base current for the second stage, while V_{CC2} supplies collector voltage and base current for the second and third stage, respectively. L_2 and L_3 are employed for both matching elements and RF chokes, while C_2 and C_3 serve as matching components as well as blocking capacitors. Base current for the first stage and collector voltage for the third stage are

supplied from the input and output port, respectively. The chip size is $1.15 \times 0.84 \text{ mm}^2$ as shown in Fig. 10(b). The area per stage is 0.32 mm^2 , 60% of the single-stage amplifier. The measurement result is shown in Fig. 10(c). The peak gain is 12.6 dB, occurring at 11.1 GHz. The input and output return losses are found to be between -10 dB and -15 dB. Ripples can be seen in the plots. These may be attributed to either extrinsic or intrinsic factors. Extrinsic factors usually involve the measurement environment connected to the device under test (DUT). Occasionally, the bias supply affects the operation of the circuits under test if the isolation of the bias probes is poor. RF choke and bypass capacitors have been employed to isolate the amplifiers under study from the bias probes. This technique may provide insufficient isolation, leading to fluctuations arising from the loading effect. Intrinsic factors are closely related to the stability of the amplifier, which was taken into account in the design to avoid the unstable region in the determination of matching points for each stage. However, process variations may have changed the S-parameters of active devices, resulting in the shift of stability circles on the Γ plane. Extracted stability factor K and $|\Delta|$ ($\Delta = S_{11}S_{22} - S_{21}S_{12}$) of the amplifier indicate the unconditional stability of the circuit in the whole band, but this does not 100% guarantee the stability of individual stages. Further investigation is necessary to locate the exact source of the fluctuations.

V. Conclusion

X- and Ku-band amplifiers, based on Si/SiGe HBTs and a novel micromachined passive component technology have been designed, fabricated, and characterized. The fabricated double mesa structure Si/SiGe HBT ($A_E = 5 \times 5 \text{ } \mu\text{m}^2$) exhibited a DC current gain of 109, and f_T and f_{max} of 28 and 52 GHz, respectively. Micromachined spiral inductors demonstrated improved resonance

frequency by a factor of more than 2, compared with devices made with conventional processing. This broadens the applicable frequency range of lumped component circuits, leading to reduced chip size at high frequencies. Characteristics of capacitors, resistors, and line sections have also been investigated. Modeling of fabricated active and passive components was carried out with appropriate equivalent circuits and applied to the design of X-band and Ku-band amplifiers. X-band single-stage amplifiers exhibit a peak gain of 4.0 dB at 10.0 GHz, while dual- and three-stage amplifiers exhibit peak gains of 5.7 dB at 10.0 GHz and 12.6 dB at 11.1 GHz, respectively. Ku-band amplifier showed a peak gain of 1.4 dB at 16.6 GHz. Minimum circuit area per stage was obtained from three-stage amplifier as 0.32 mm^2 in X-band.

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Figure Captions

Figure 1. Si/SiGe HBT material structure.

Figure 2. Orientation dependence of KOH etching profile. A-B: aligned for (110) orientation. C-D: aligned for (100) orientation.

Figure 3. (a) Measured current-voltage characteristics of the Si/SiGe HBT with emitter size of $5 \times 5 \mu\text{m}^2$; (b) Measured Gummel plot of the HBT ($A_E = 5 \times 5 \mu\text{m}^2$) with DC current gain β in the inset. Current gain is measured with $V_{CE} = 4 \text{ V}$; (c) $|H_{21}|$ and U of the HBT ($A_E = 5 \times 5 \mu\text{m}^2$) measured at $I_C = 7.0 \text{ mA}$ and $V_{CE} = 4.0 \text{ V}$. $f_T = 28 \text{ GHz}$ and $f_{\text{max}} = 52 \text{ GHz}$.

Figure 4. HBT T-model small signal equivalent circuit and parameters extracted.

Figure 5. (a) Photomicrograph of the micromachined spiral inductor with etch depth of $20 \mu\text{m}$; (b) Equivalent circuit of spiral inductor. C_{P1} and C_{P2} represent parasitic capacitance between inductor and ground. C_C is parasitic coupling capacitance. R_S is parasitic series resistance. L is main inductance; (c) Resonance frequencies of inductors with various etch depth, d_{etch} .

Figure 6. (a) Equivalent circuit of MIM capacitor. C_{P1} and C_{P2} represent parasitic capacitance between capacitor and ground. R_S and L_S are parasitic series resistance and inductance, respectively. R_C is parasitic parallel resistance. C is main capacitance; (b) Equivalent circuit of resistor and line section. C_{P1} and C_{P2} represent parasitic capacitance between resistor(line section) and ground. L_S is parasitic series inductance and R is main resistance for resistor equivalent circuit. R is parasitic series resistance and L_S is main

inductance for line section equivalent circuit.

Figure 7. X-band single-stage amplifier: (a) Circuit diagram; (b) Photomicrograph of fabricated circuit. Chip size= $0.75 \times 0.65 \text{ mm}^2$; (c) Measured transducer gain S_{21} , input return loss S_{11} , and output return loss S_{22} .

Figure 8. Ku-band single-stage amplifier: (a) Measured transducer gain S_{21} , input return loss S_{11} , and output return loss S_{22} ; (b) Measured $VSWR_{in}$ and $VSWR_{out}$.

Figure 9. X-band dual-stage amplifier: (a) Circuit diagram; (b) Photomicrograph of fabricated circuit. Chip size= $0.98 \times 0.80 \text{ mm}^2$; (c) Measured transducer gain S_{21} , input return loss S_{11} , and output return loss S_{22} .

Figure 10. X-band three-stage amplifier: (a) Circuit diagram; (b) Photomicrograph of fabricated circuit. Chip size= $1.15 \times 0.84 \text{ mm}^2$; (c) Measured transducer gain S_{21} , input return loss S_{11} , and output return loss S_{22} .

n+ Si	Emitter contact	Sb $2\times 10^{19} \text{ cm}^{-3}$	2000 Å
n Si	Emitter	Sb $2\times 10^{18} \text{ cm}^{-3}$	1000 Å
i $\text{Si}_{0.6}\text{Ge}_{0.4}$			50 Å
p+ $\text{Si}_{0.6}\text{Ge}_{0.4}$	Base	B $2\times 10^{19} \text{ cm}^{-3}$	200 Å
i $\text{Si}_{0.6}\text{Ge}_{0.4}$			50 Å
n- Si	Collector	Sb $5\times 10^{15} \text{ cm}^{-3}$	3000 Å
n+ Si	Sub-collector	As $1\times 10^{19} \text{ cm}^{-3}$	15000 Å
p- Si	Substrate	$1\times 10^{12} \text{ cm}^{-3}$	540 µm

Figure 1

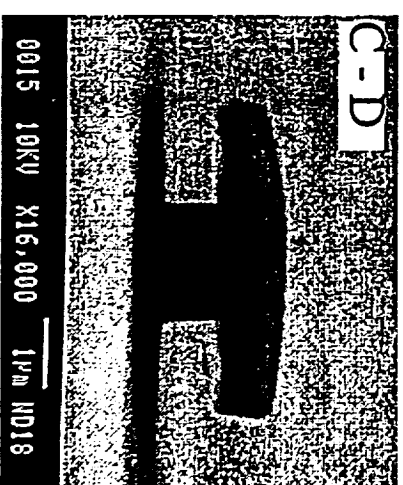
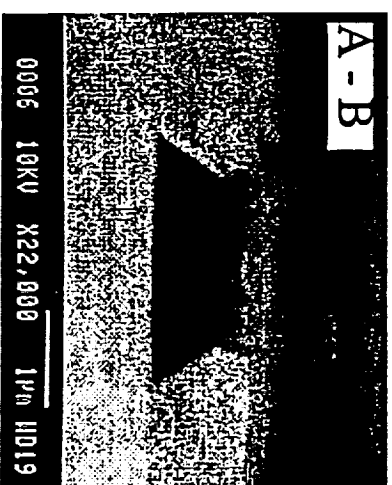
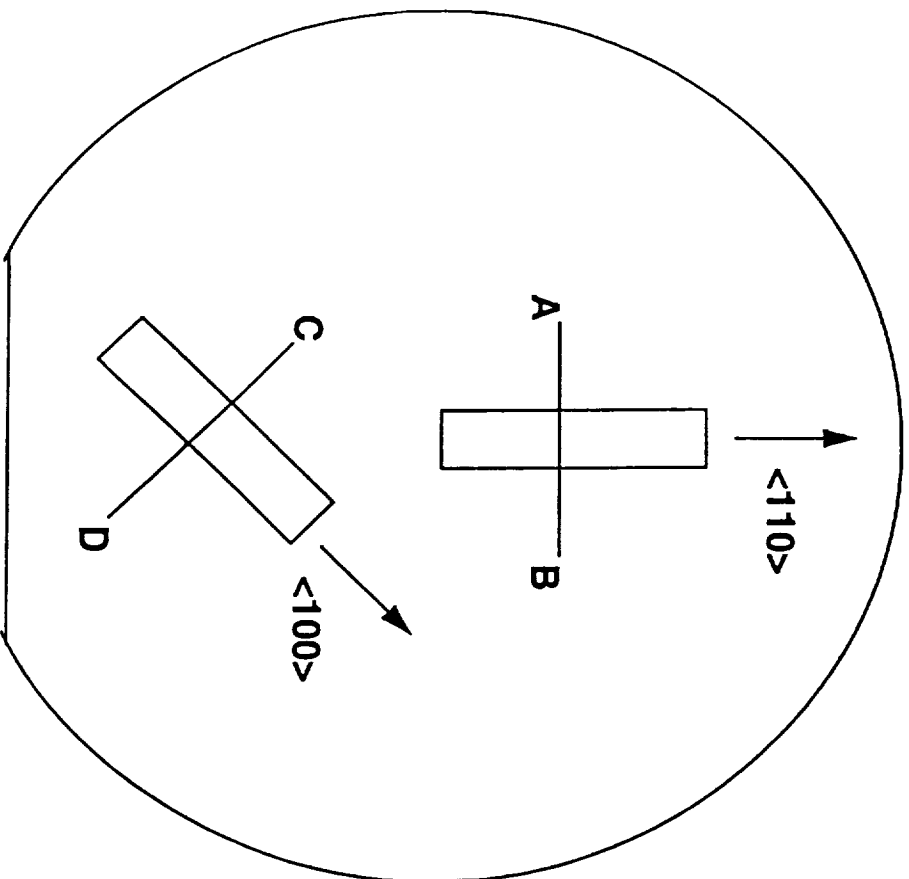


Figure 2

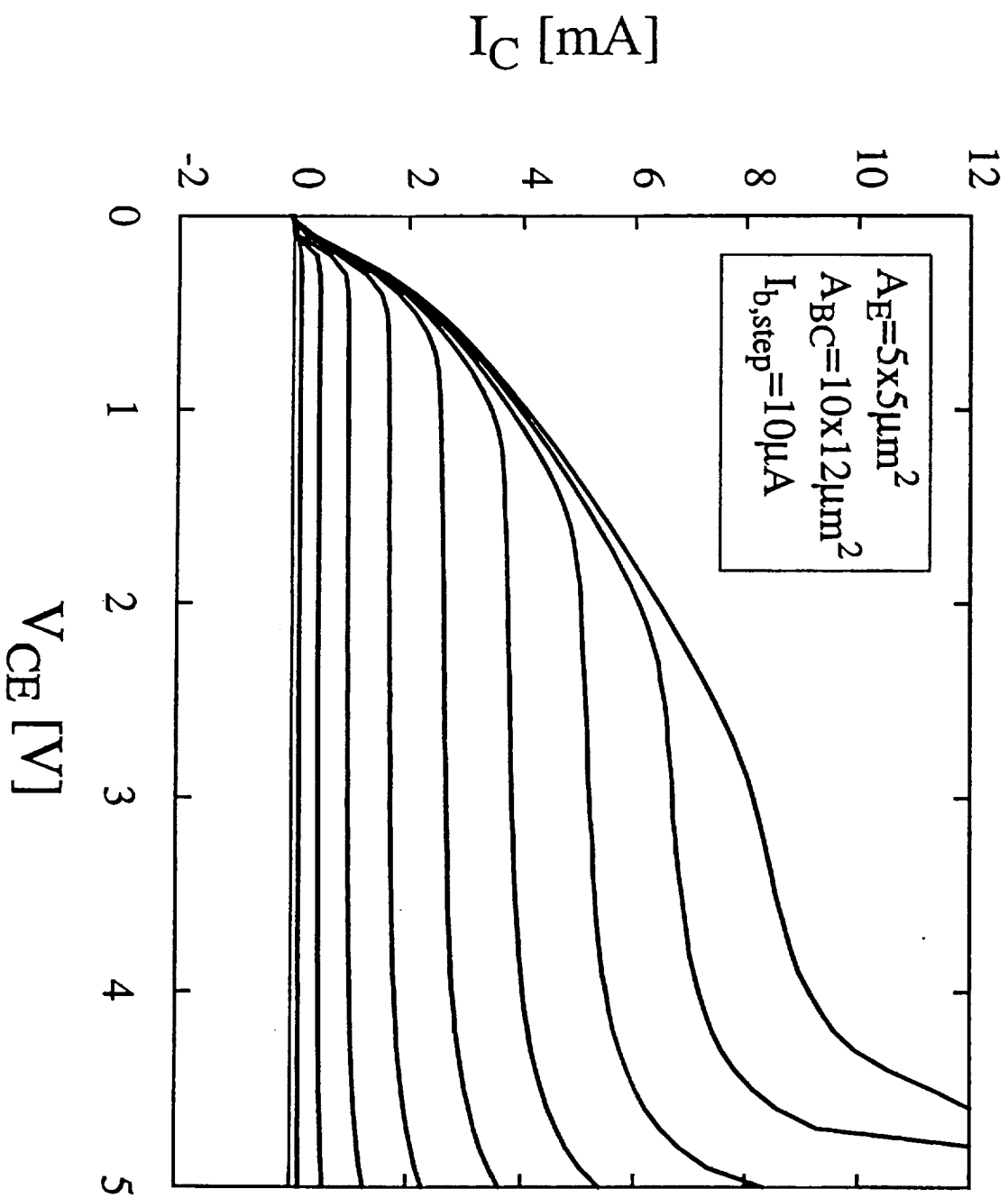


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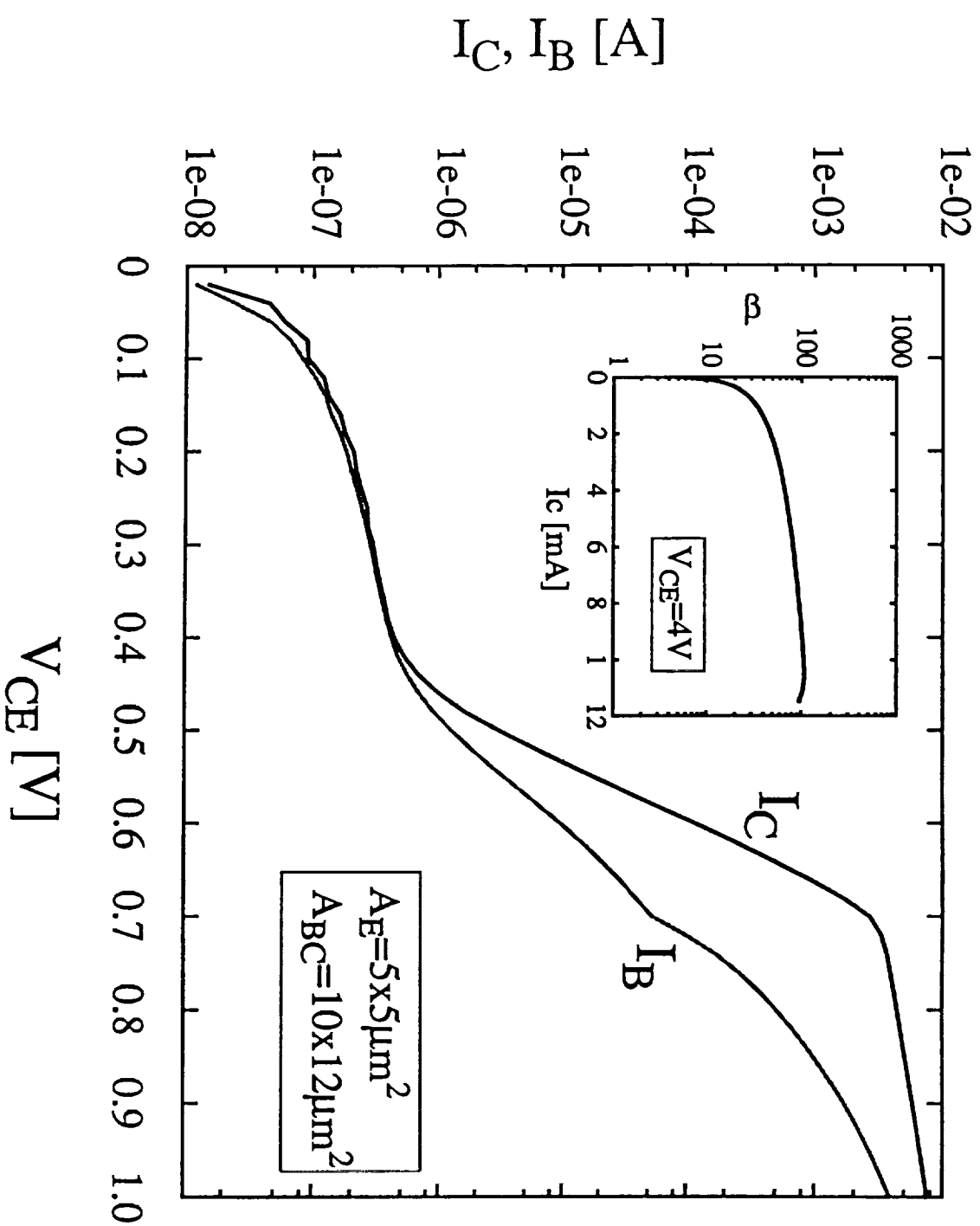


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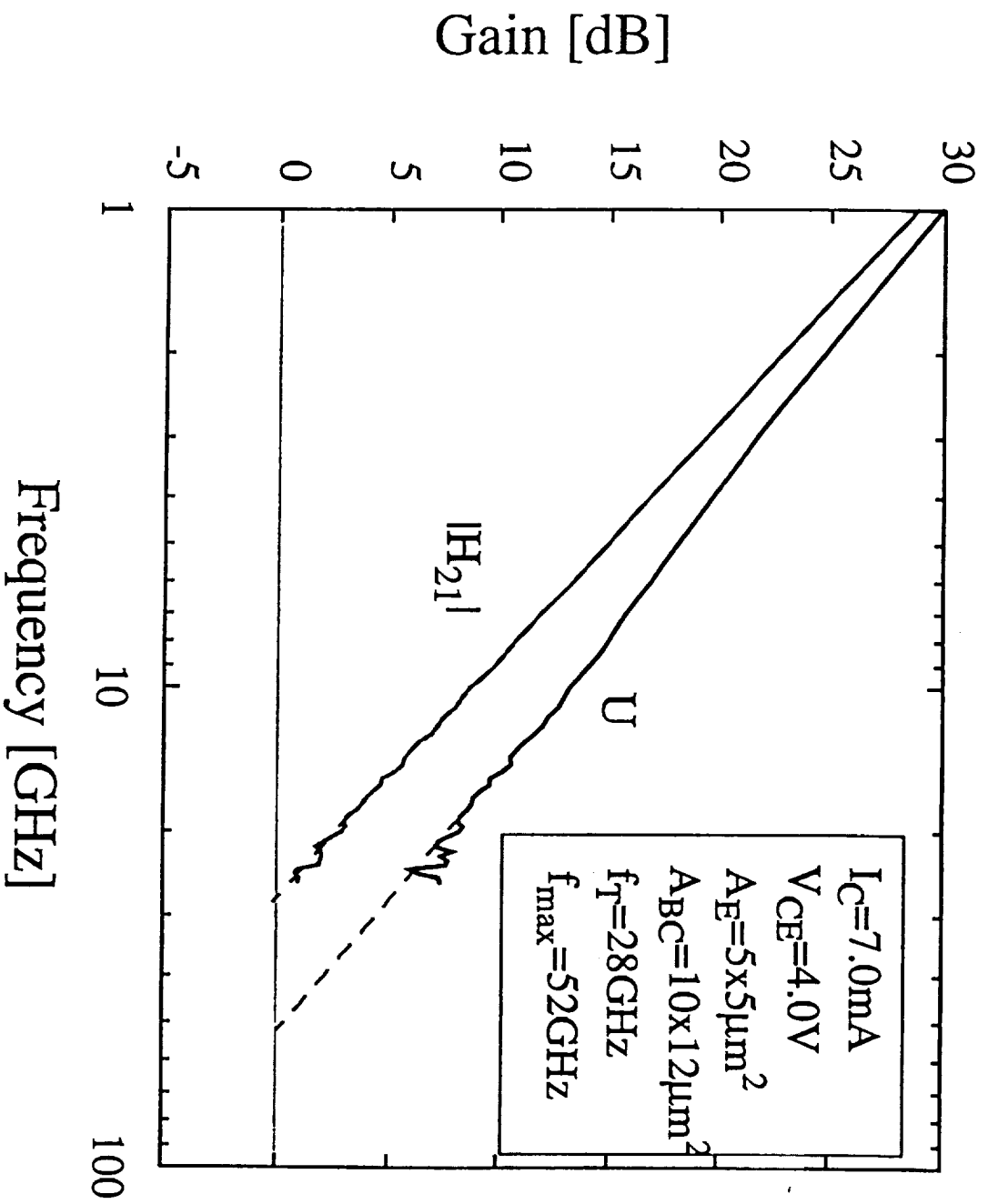
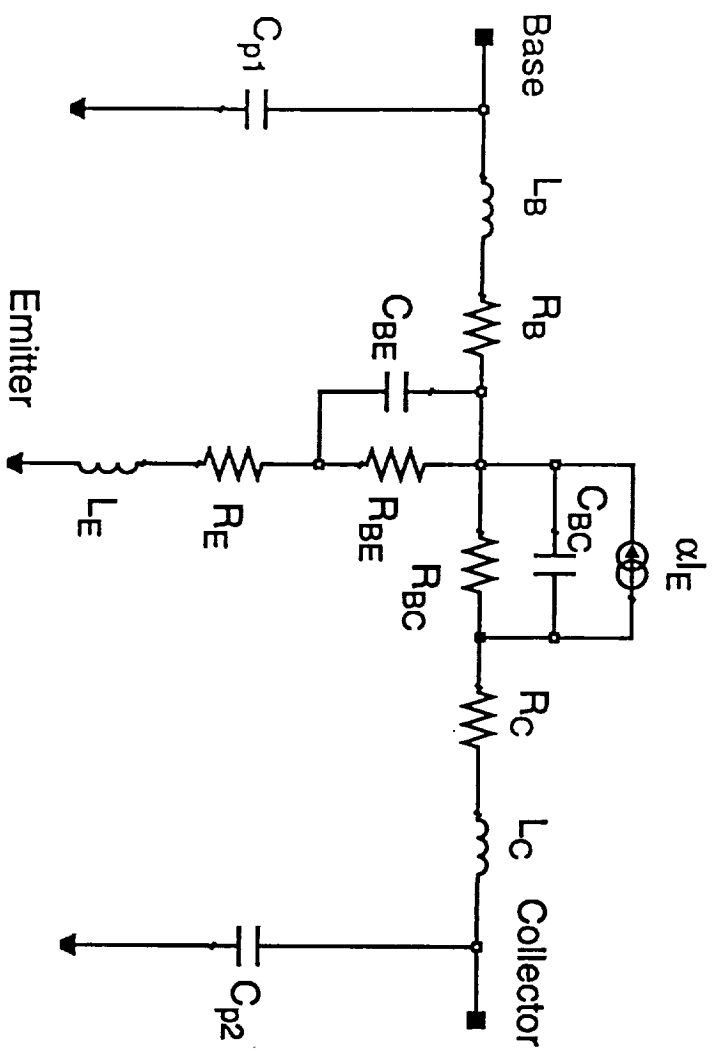


Figure 3 (c)



R_B	13.1 Ω
L_B	62.6 pH
R_{BE}	1.0 Ω
C_{BE}	106.8 fF
R_E	15.8 Ω
L_E	141.7 pH
R_{BC}	127.0 k Ω
C_{BC}	28.9 fF
R_C	24.8 Ω
L_C	66.1 pH
$C_{p1,2}$	4.0 fF
α_o	0.995

Figure 4

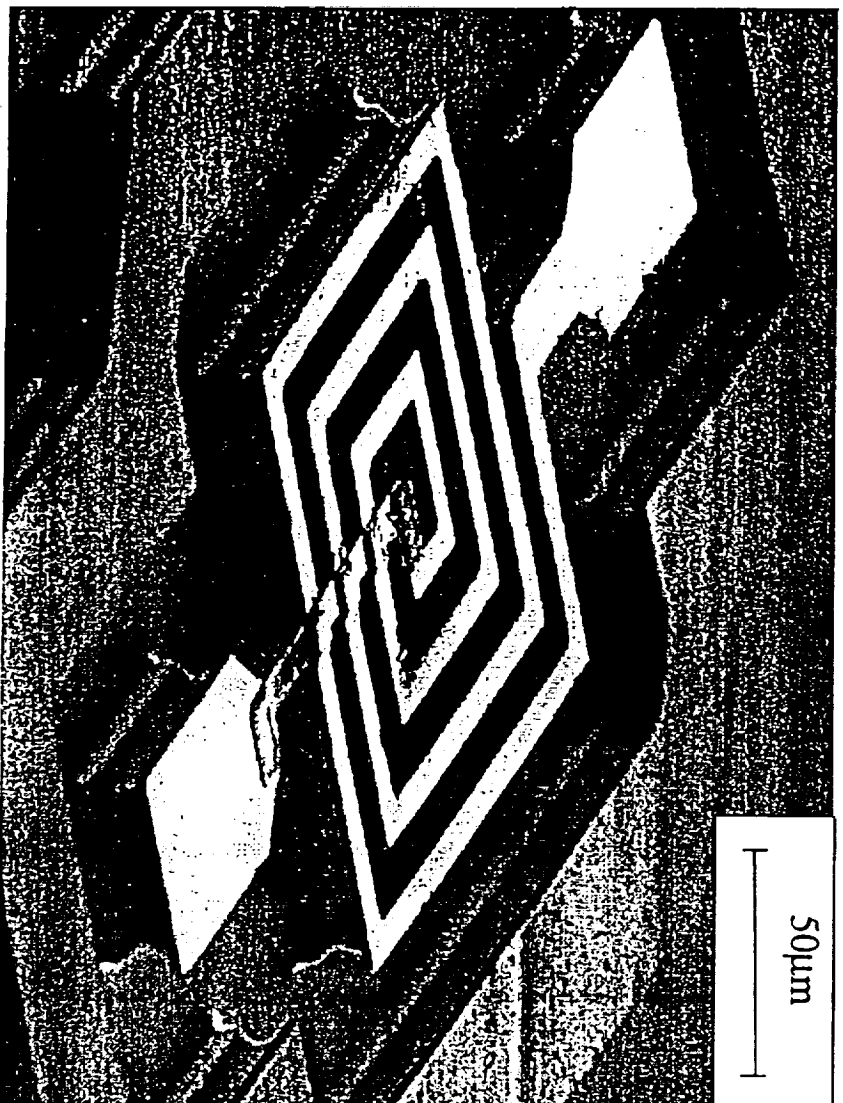


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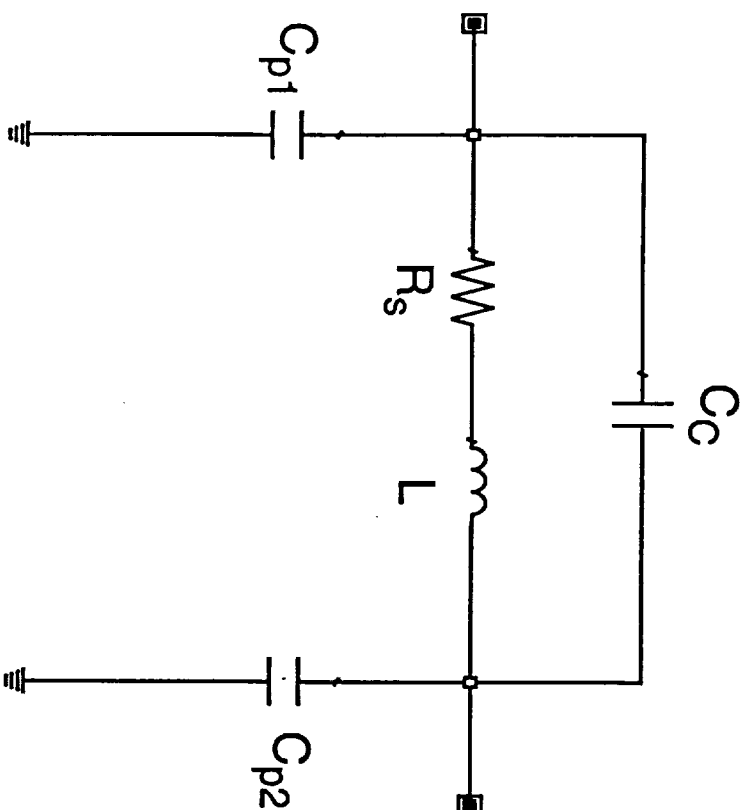


Figure 5(b)

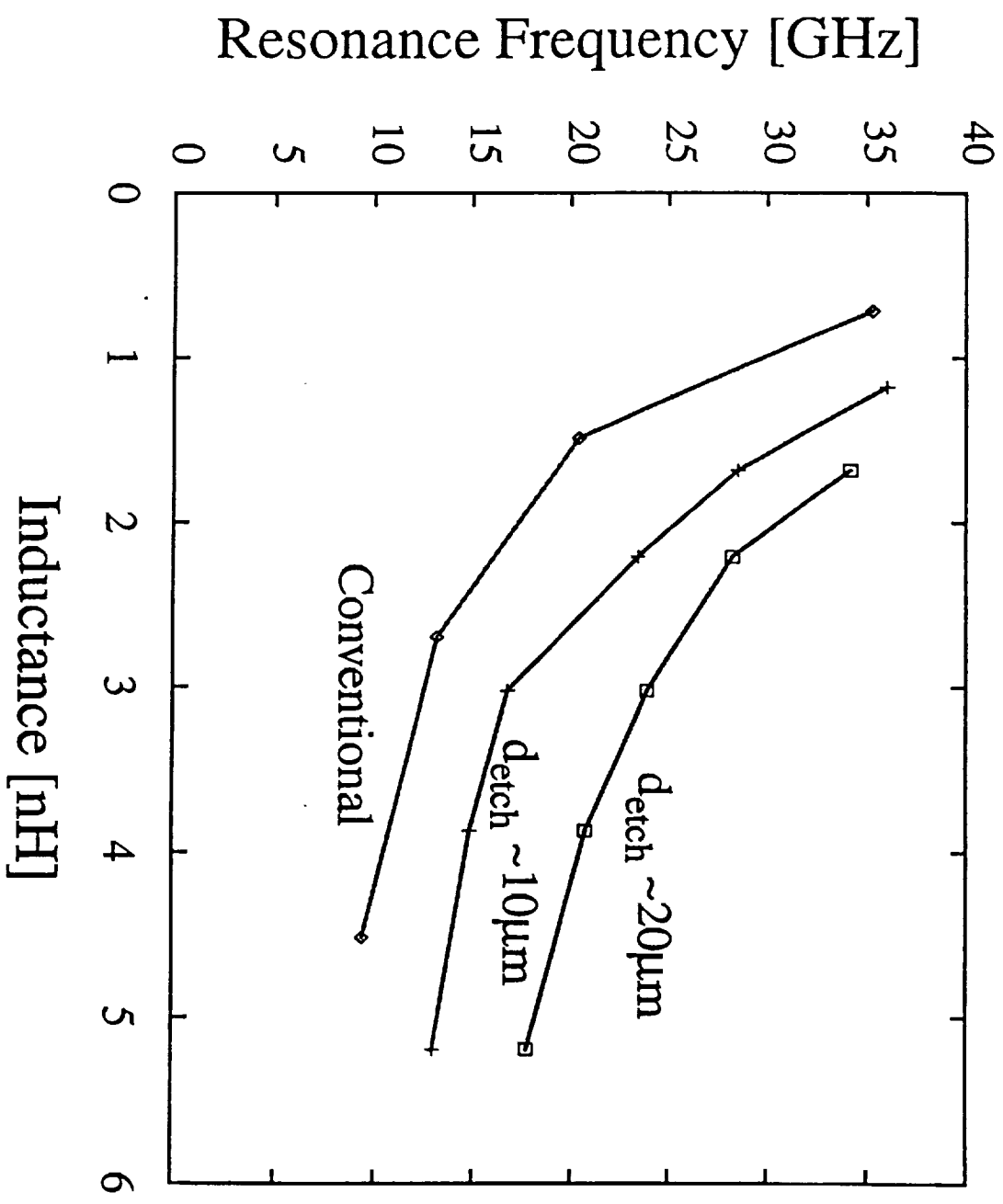


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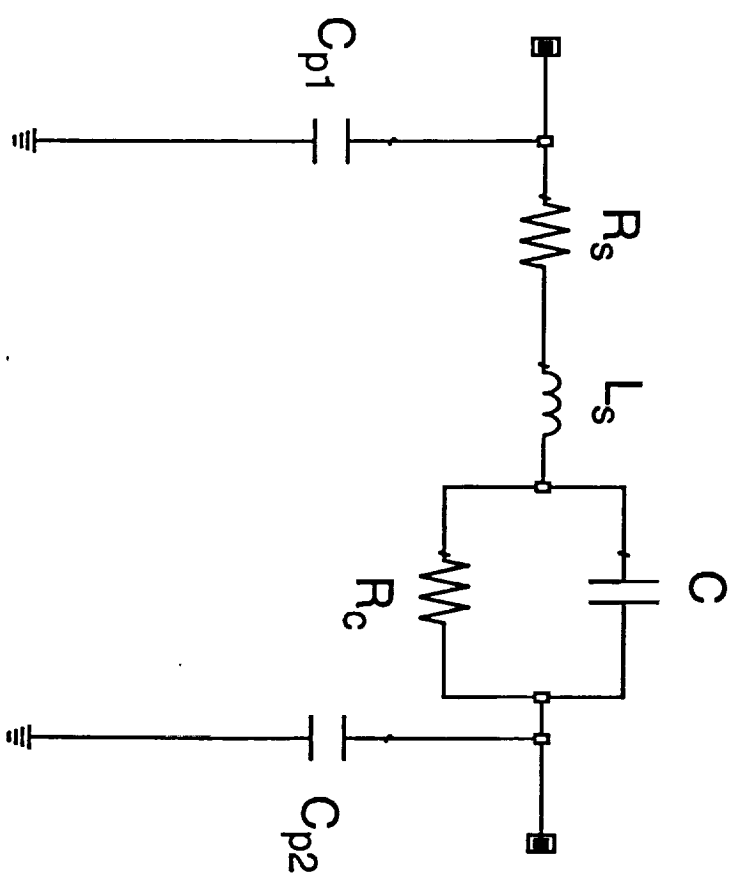


Figure 6(a)

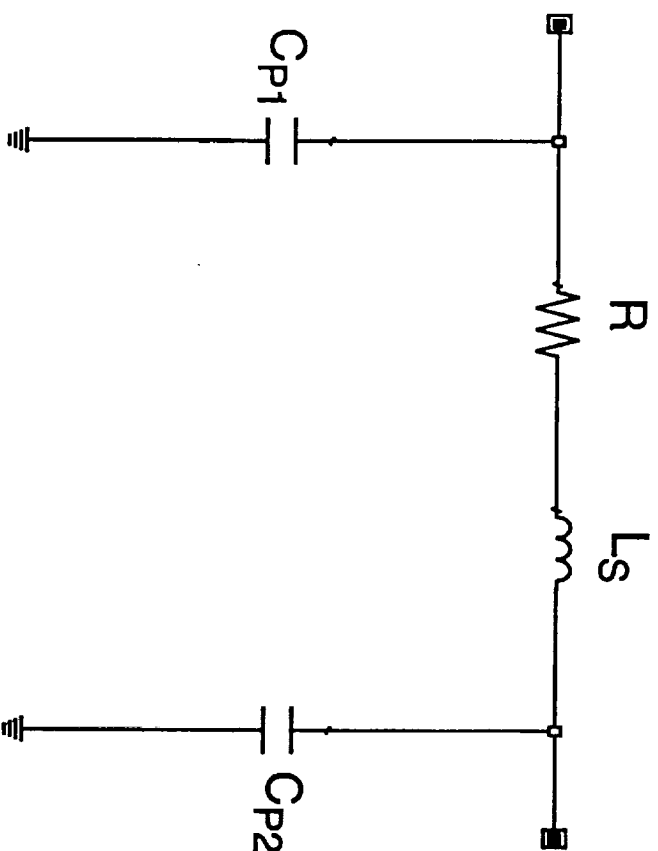


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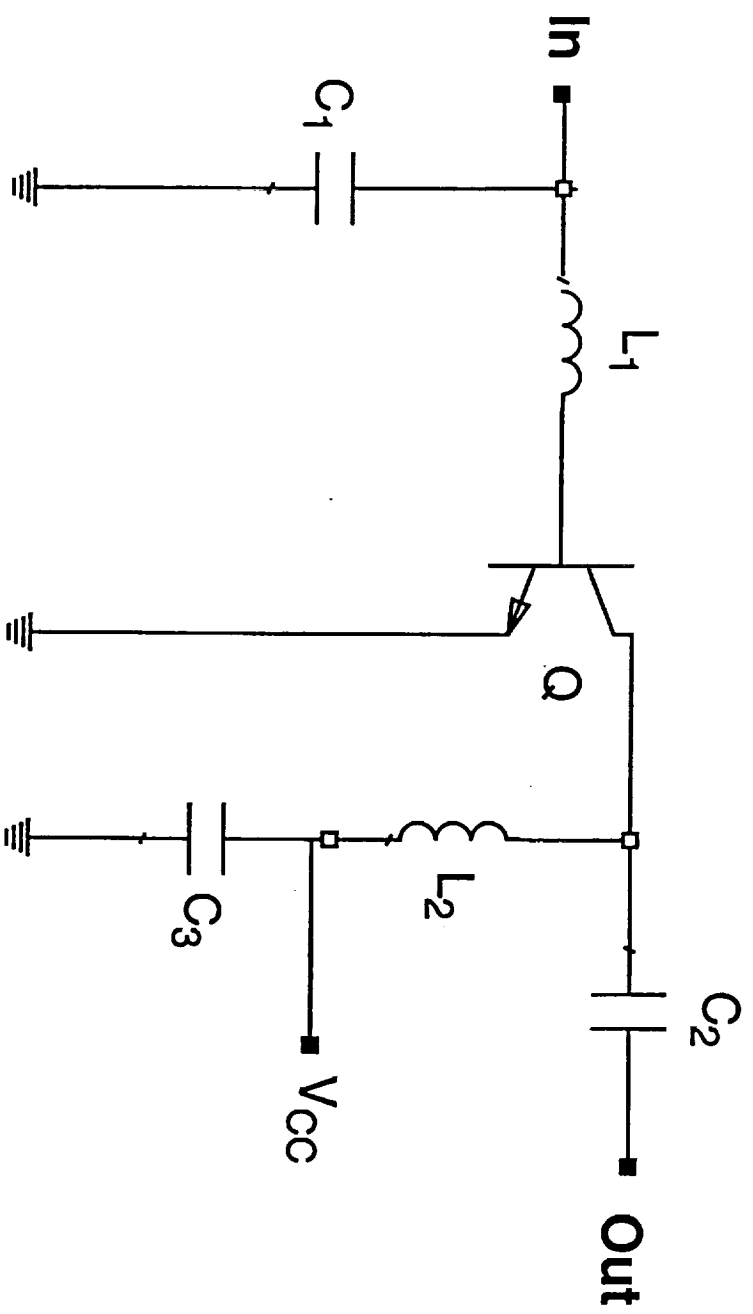


Figure 7(a)

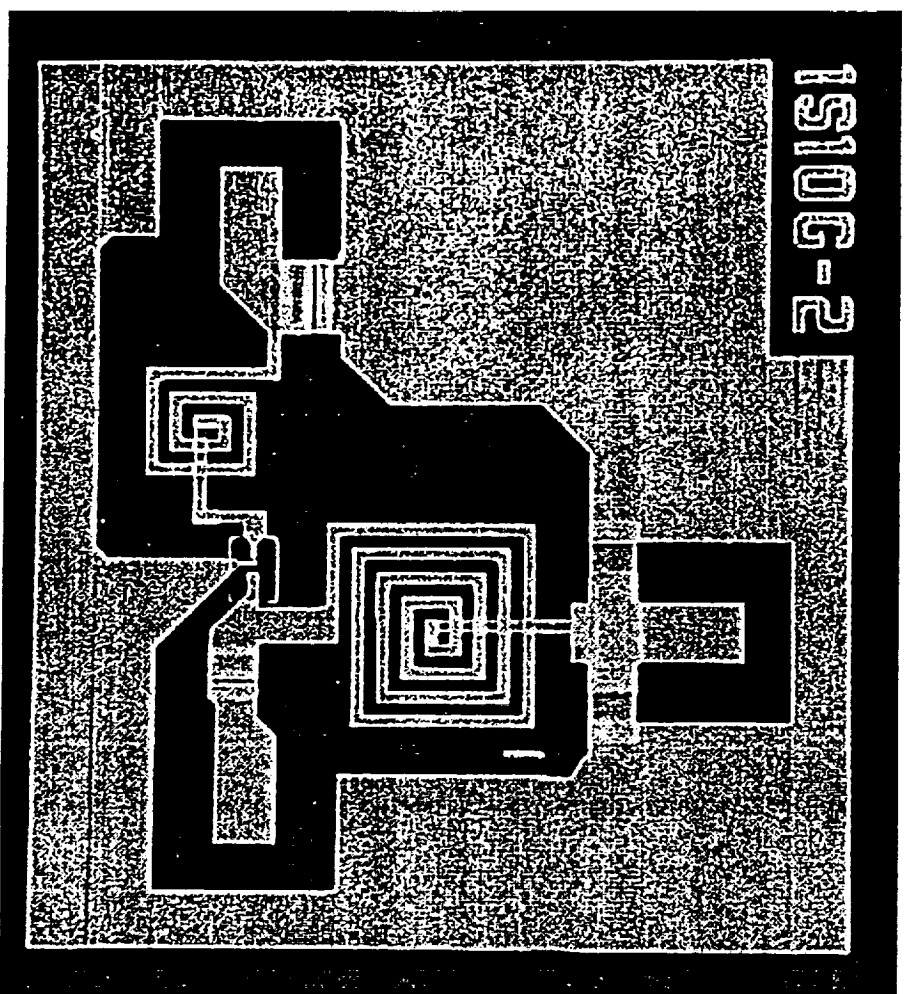


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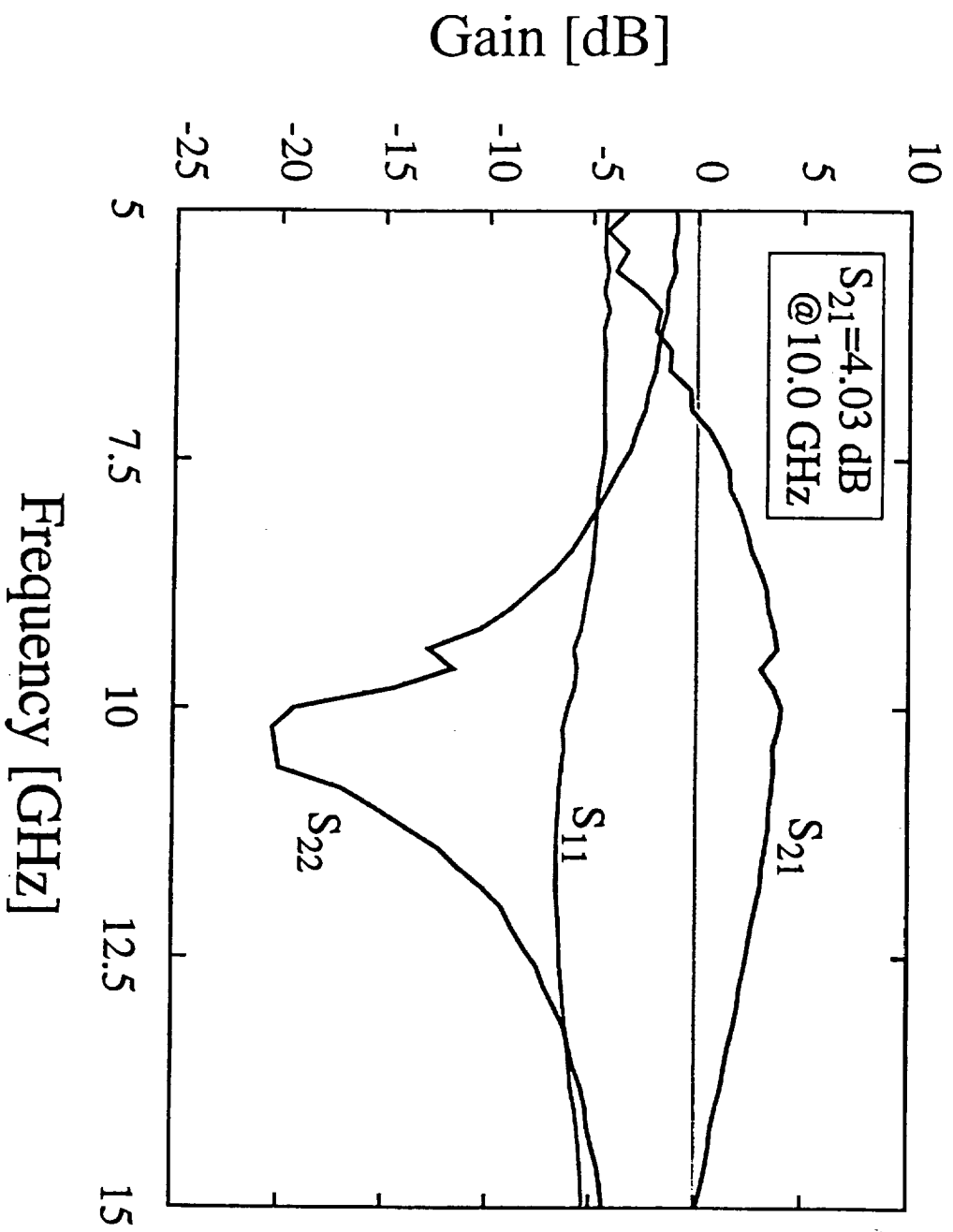


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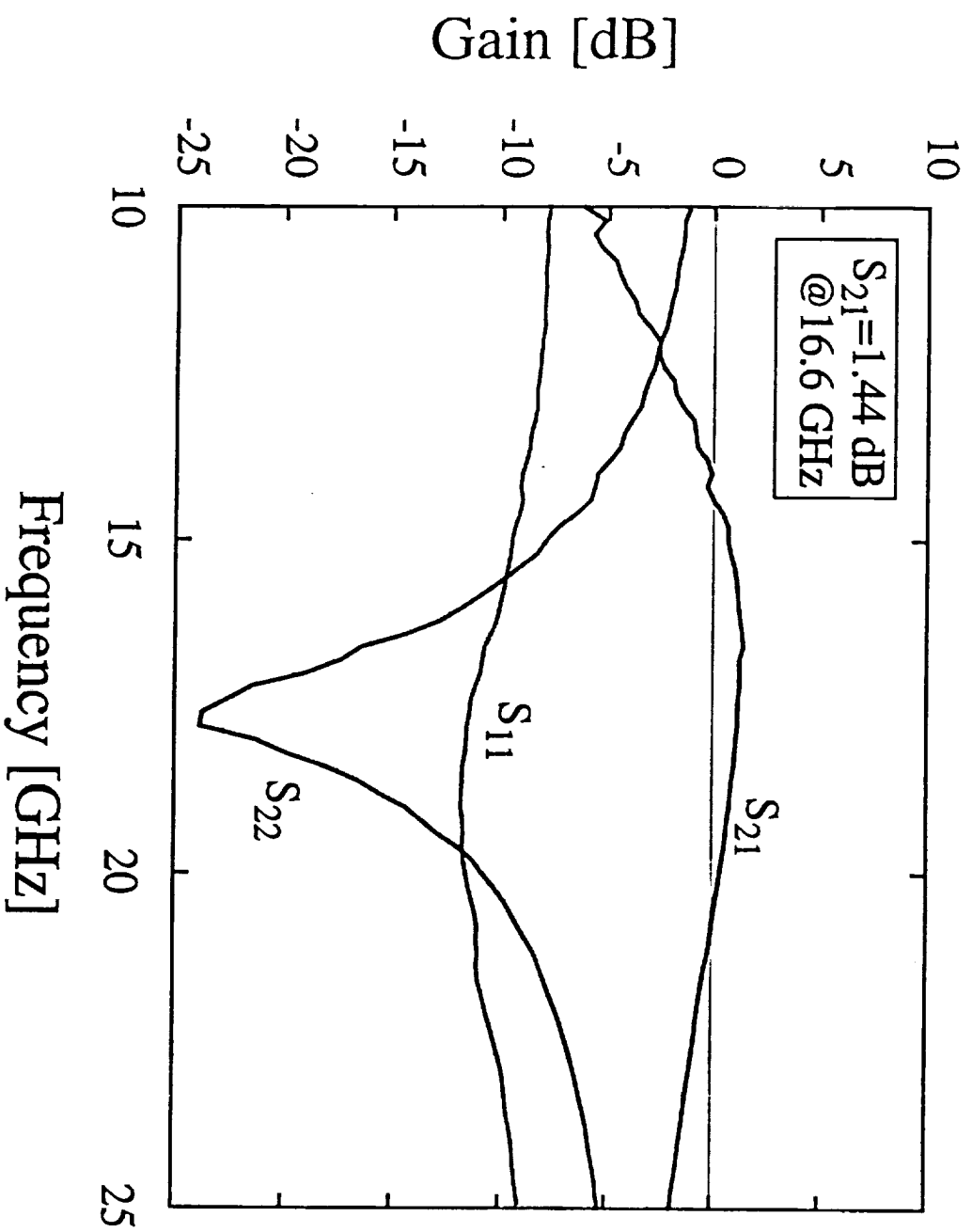


Figure 8(a)

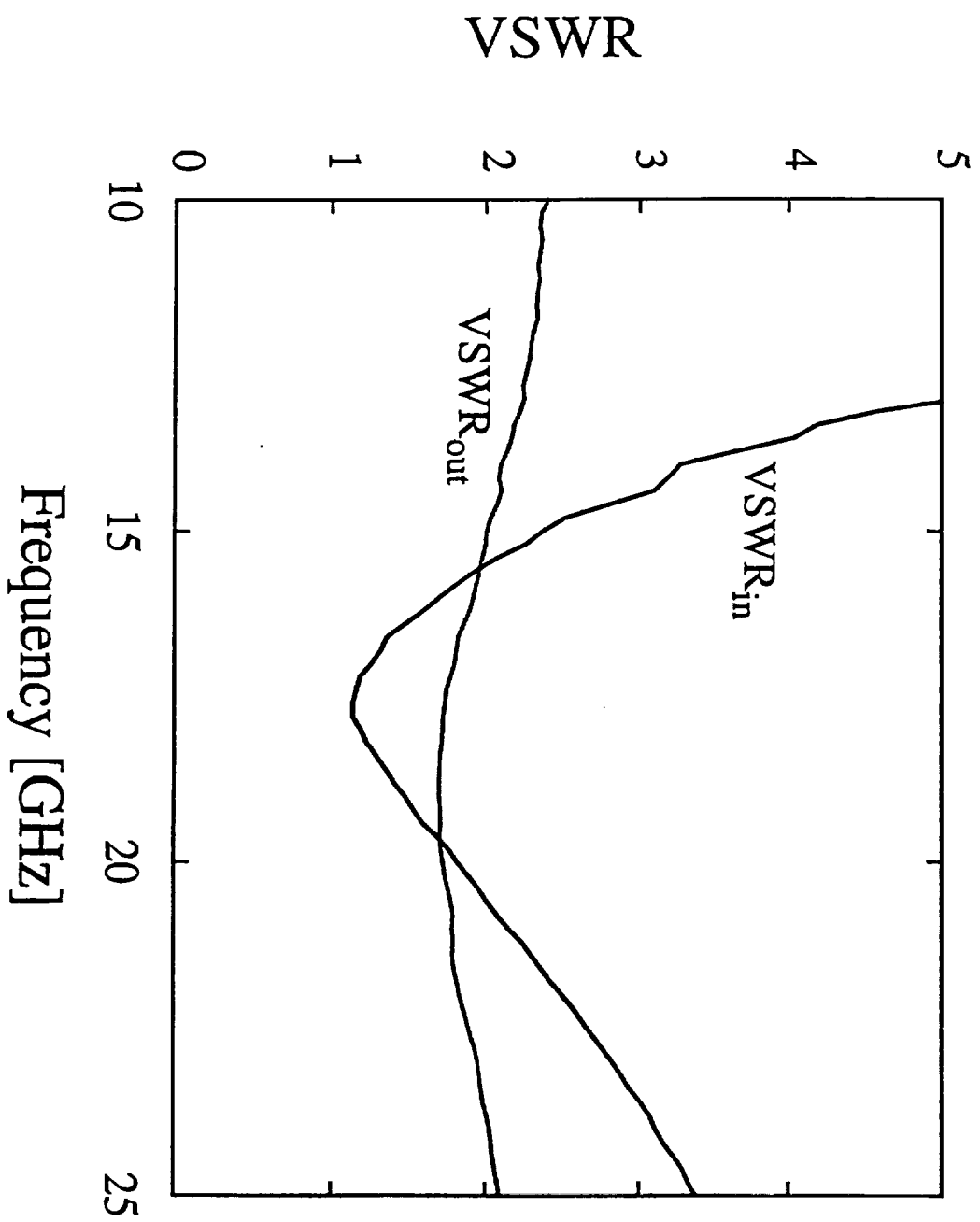


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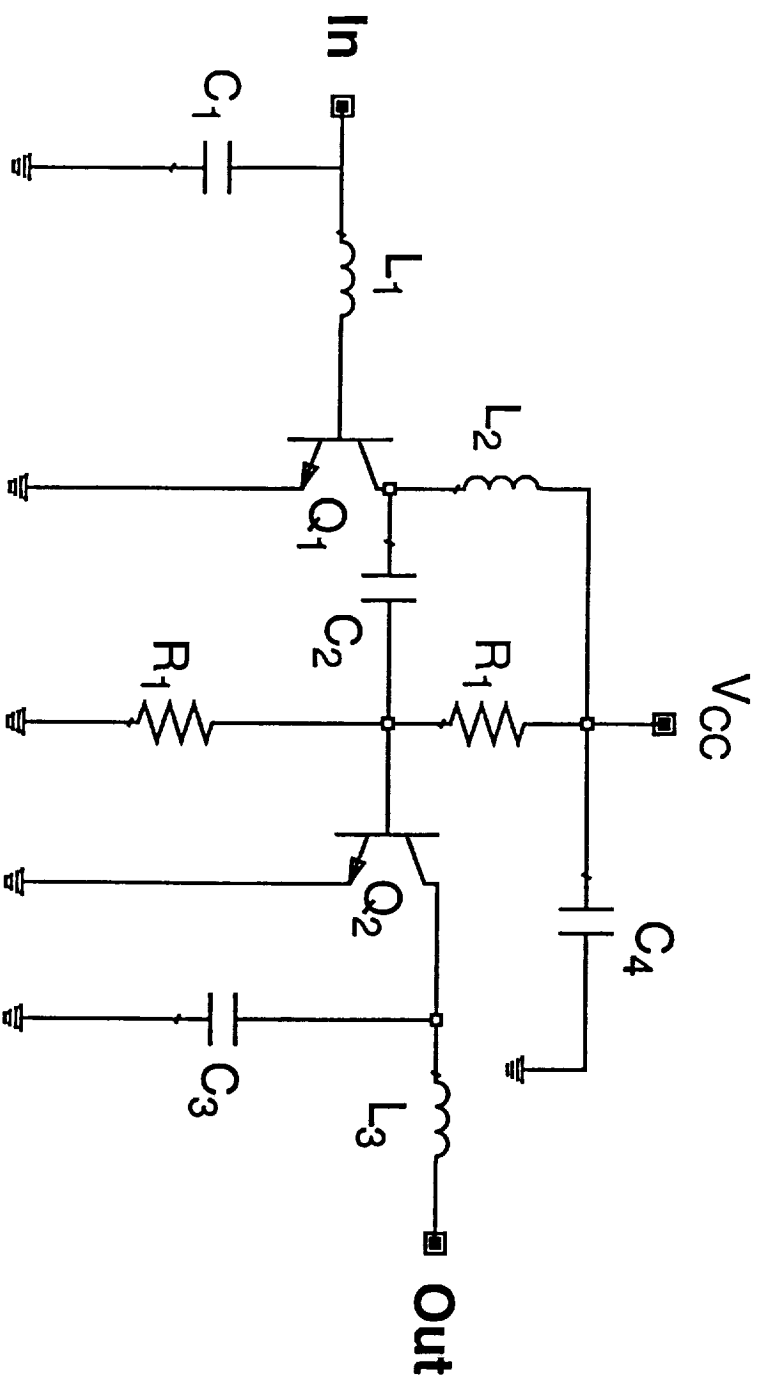


Figure 9(a)

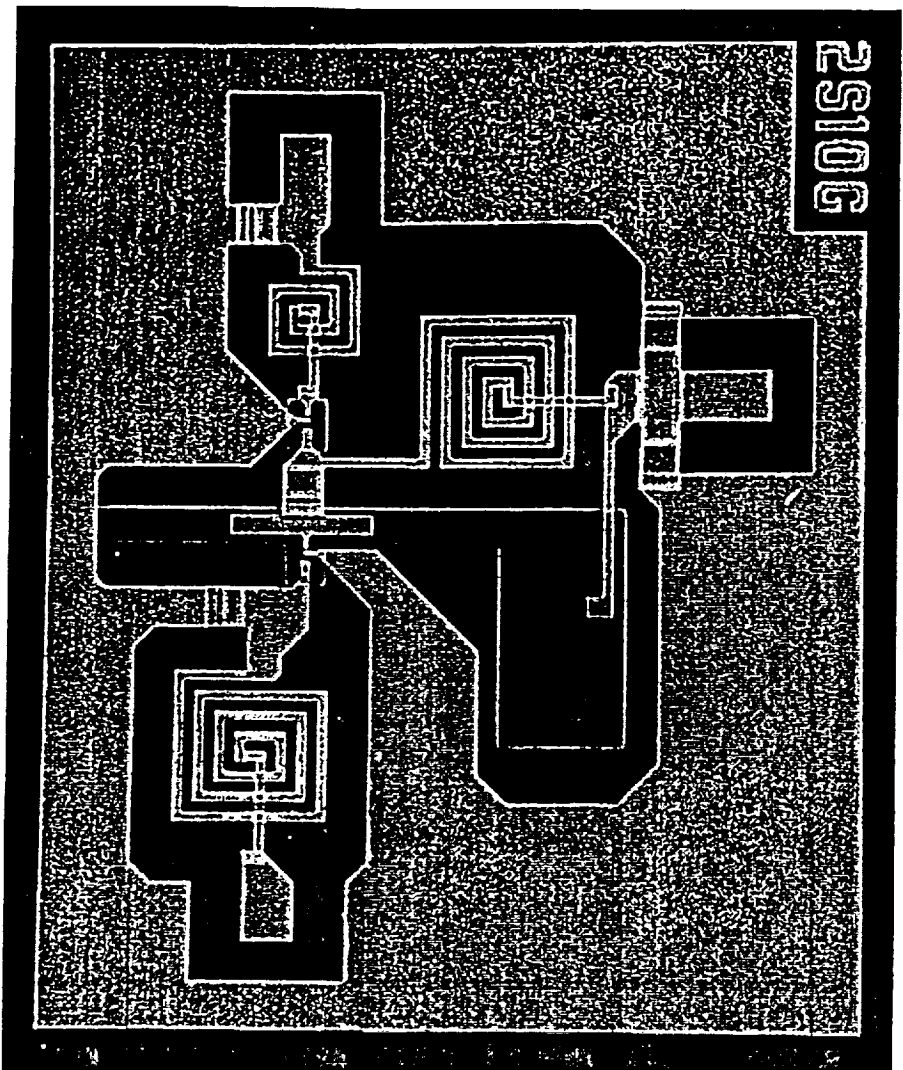


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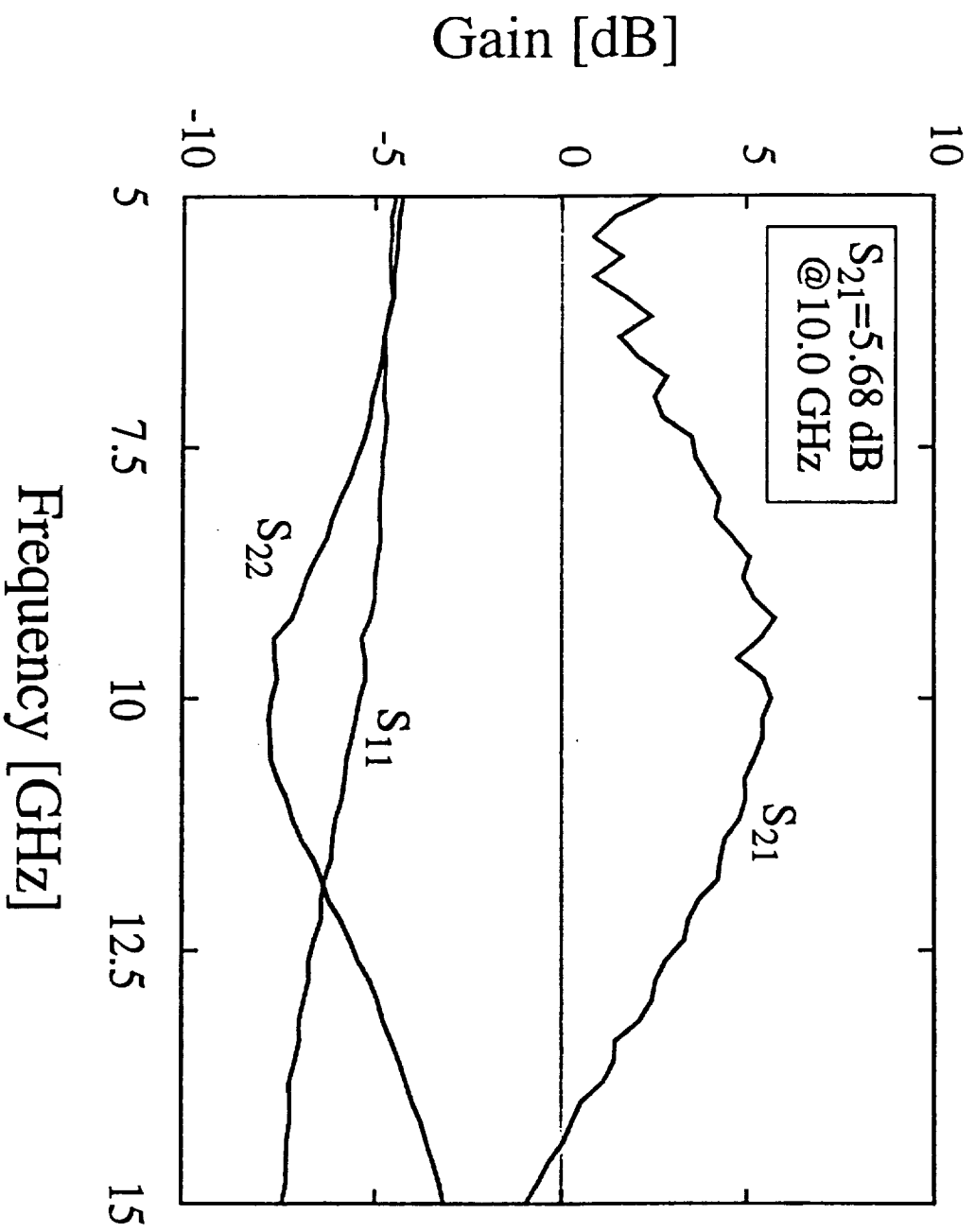


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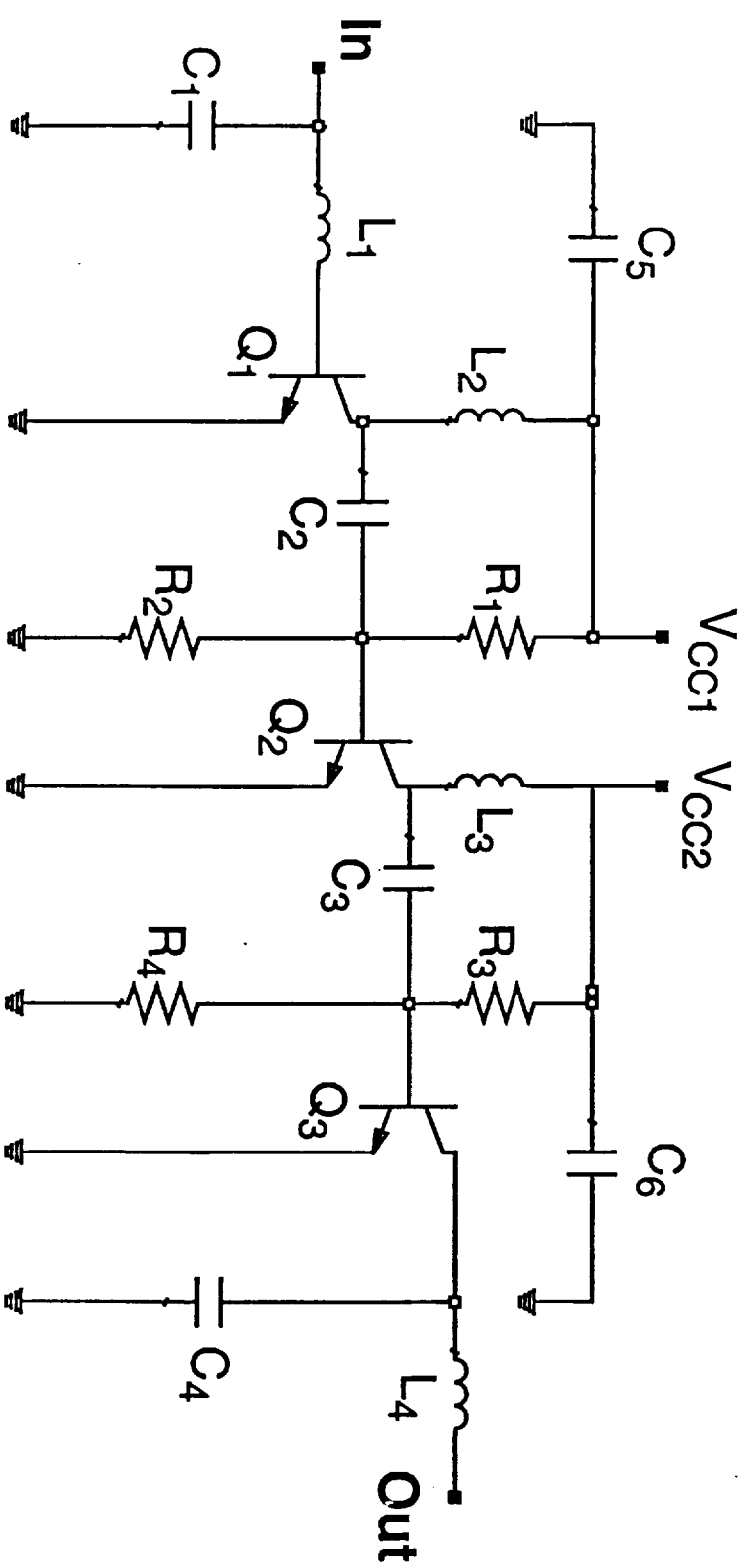


Figure 10(a)

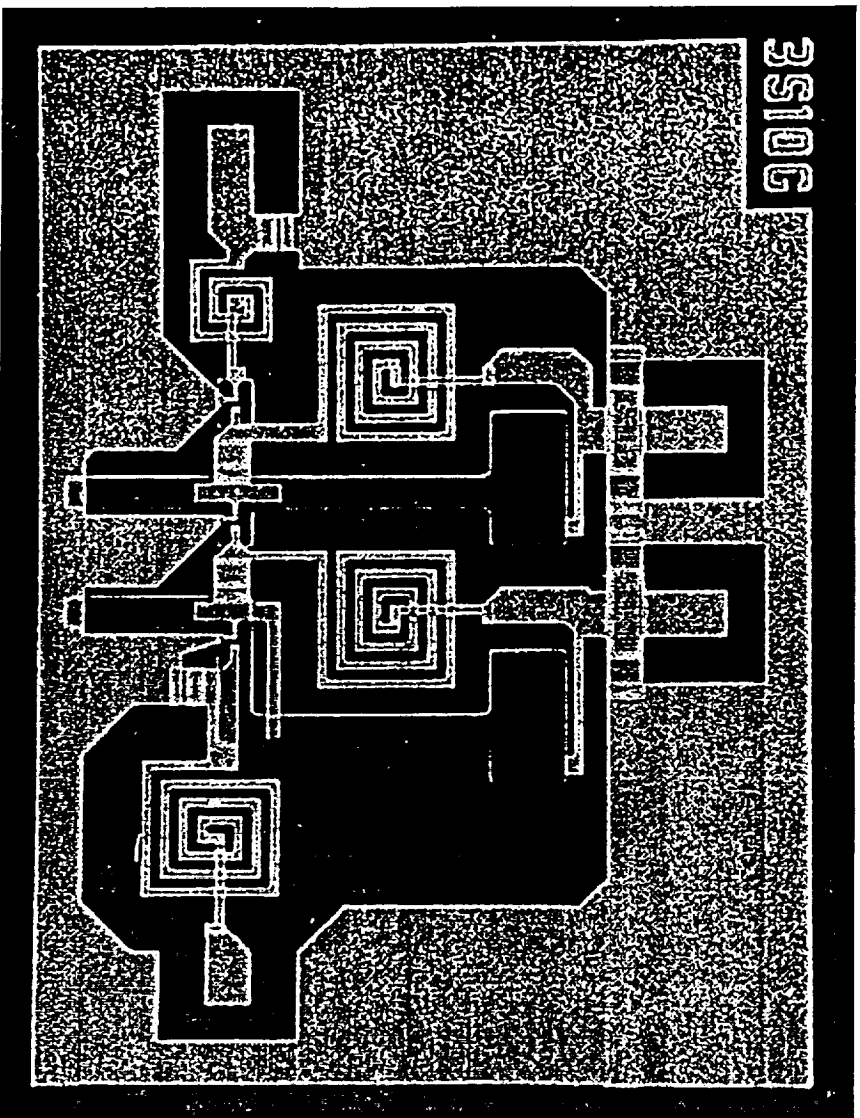


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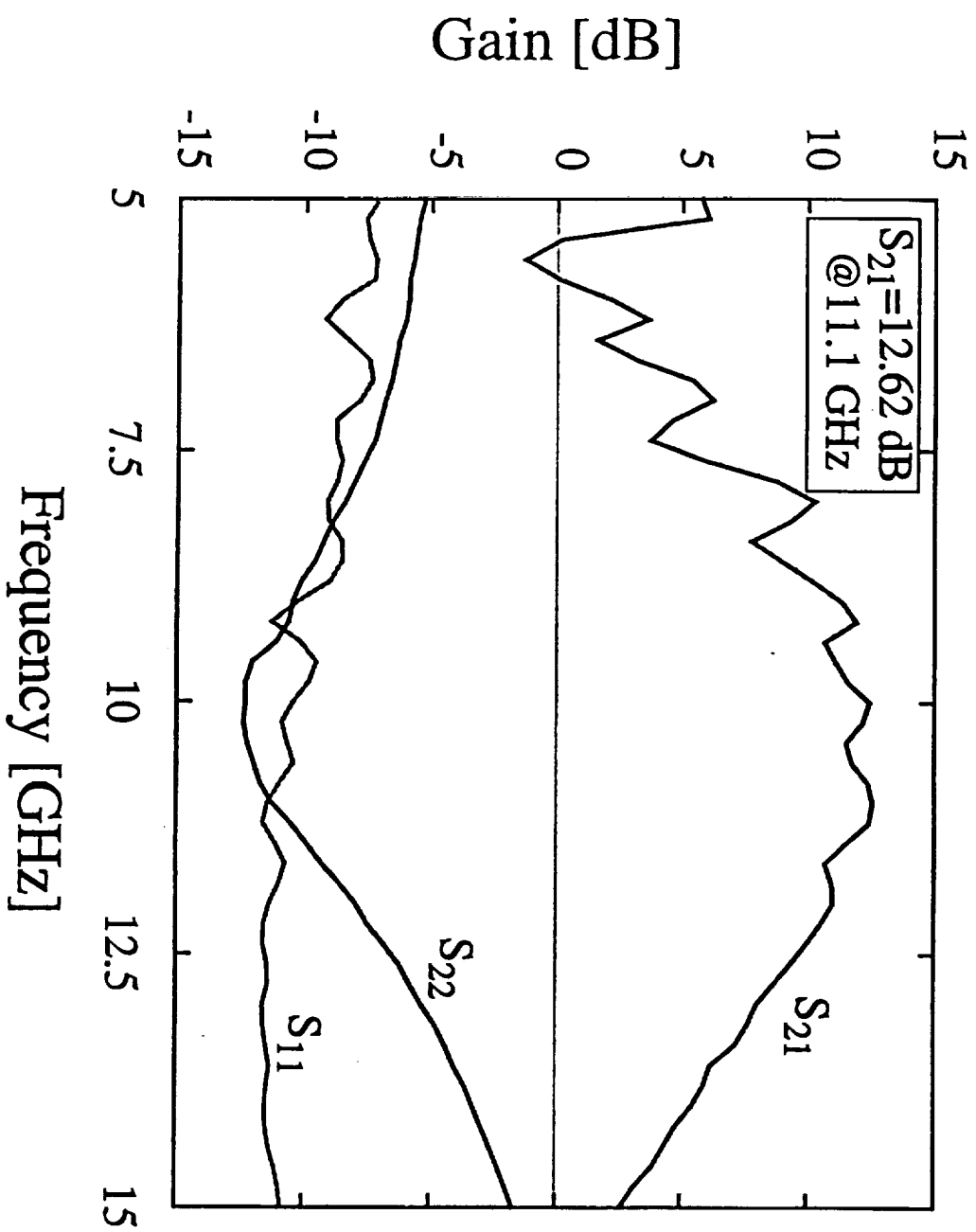


Figure 10(c)